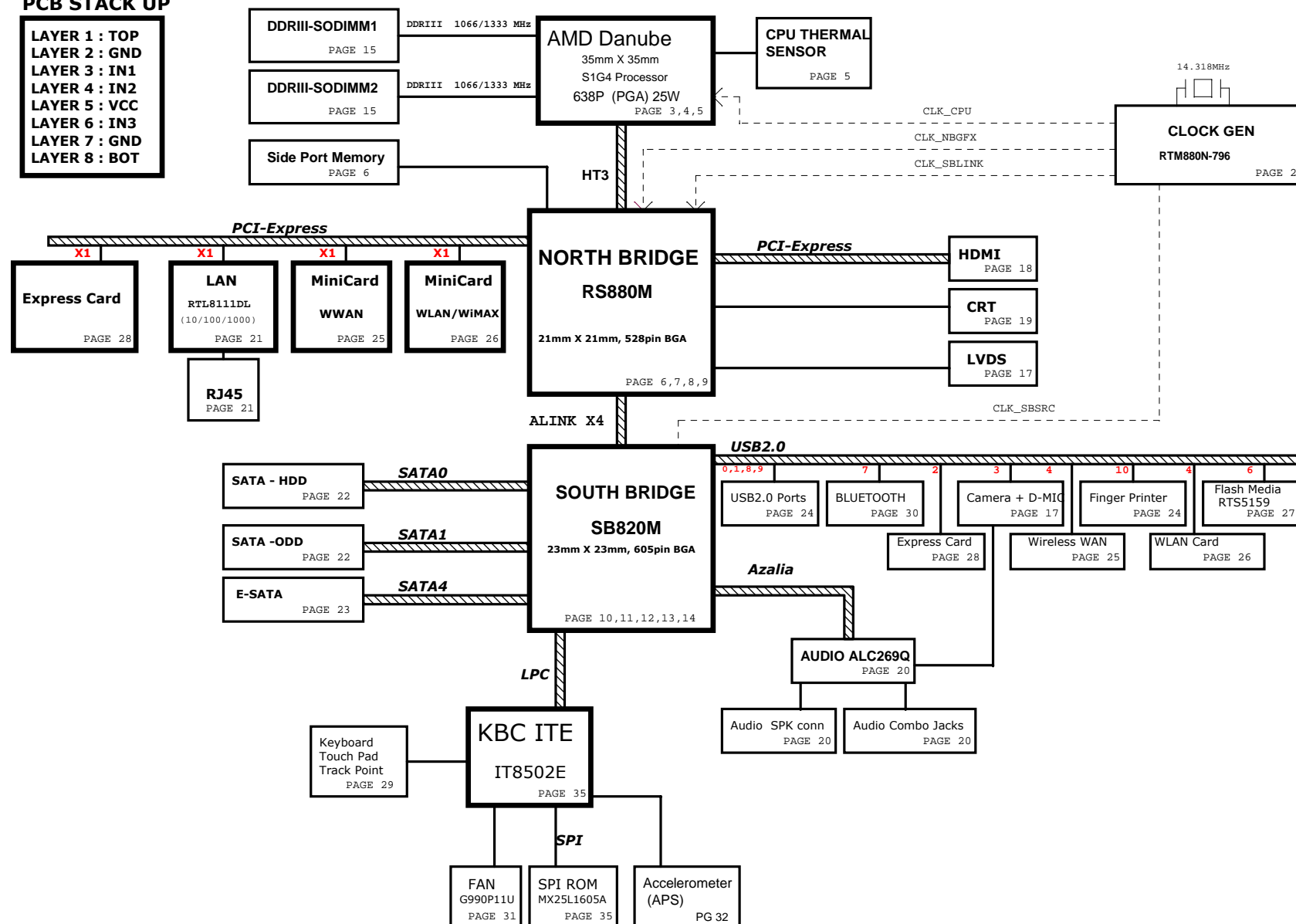


LD-Note Block Diagram -- AMD Danube

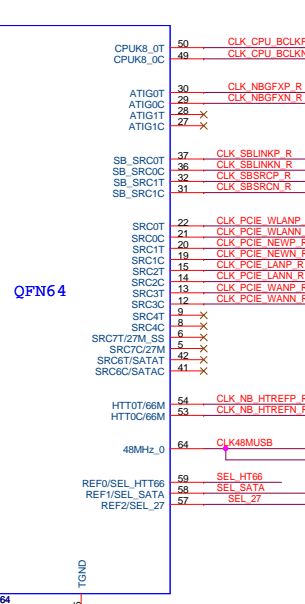
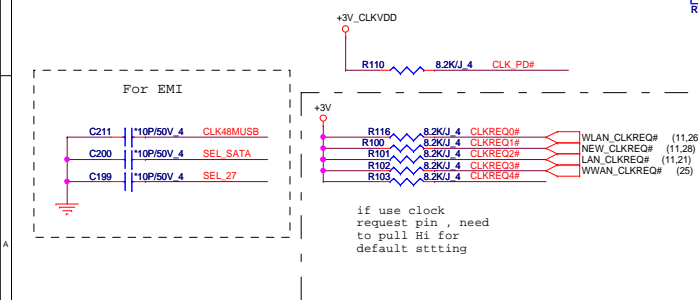
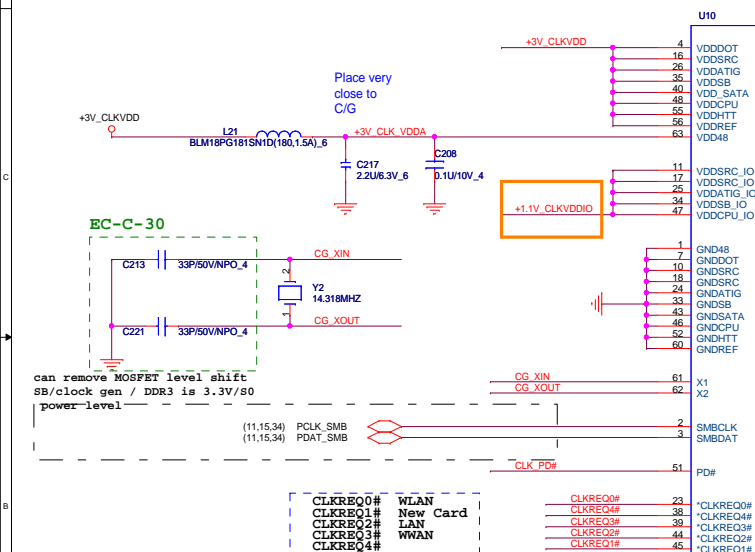
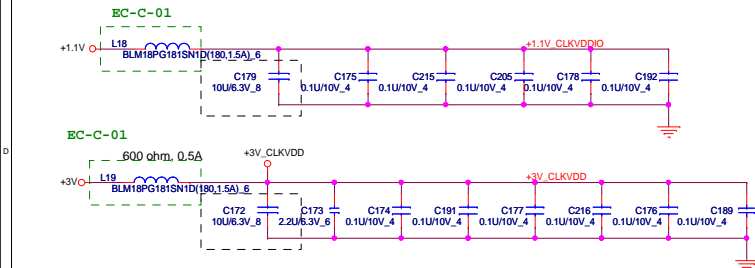
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



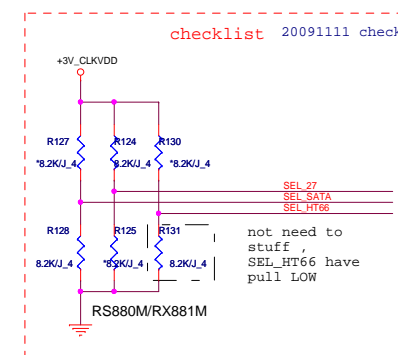
CLOCKS name	Discrete	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP48 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP47 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R213, R215 STUFF	To Park-S3 27Mhz - Discrete only

Need check the net name for the short pad

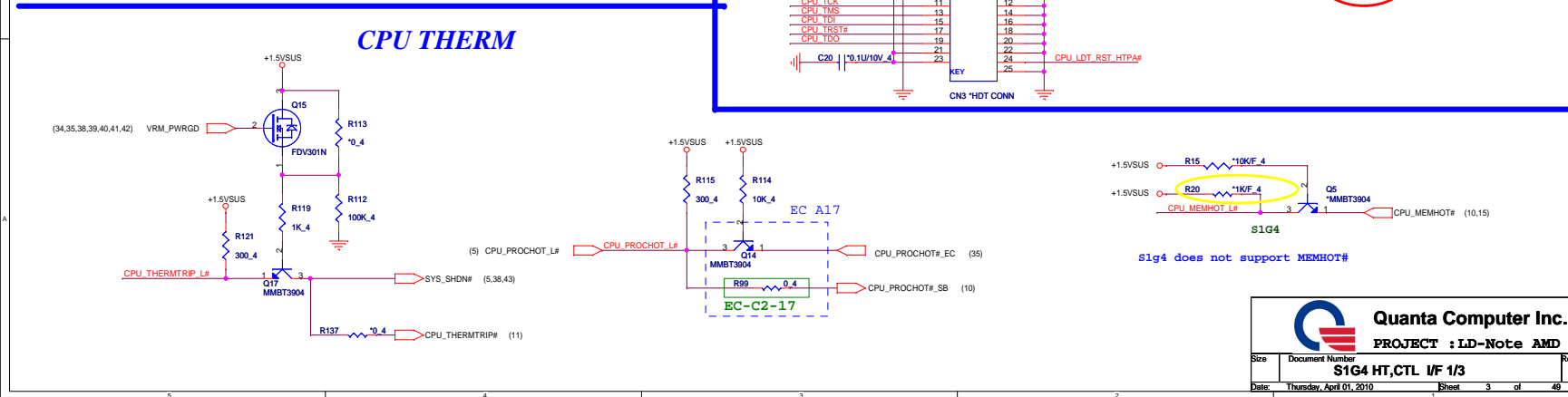


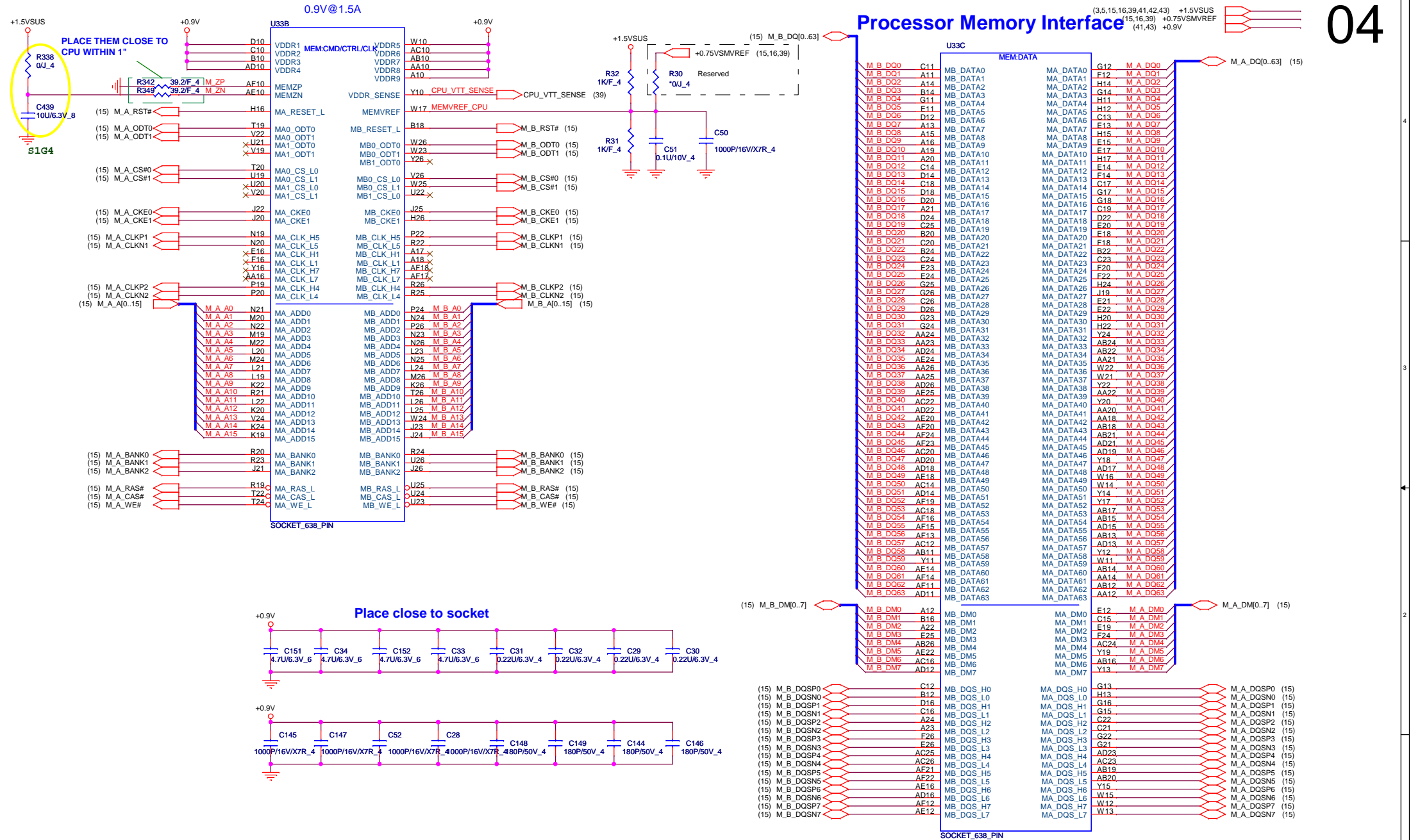
IDT ICS9LPRS476AKLFT
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796--AL000880001

* default	
SEL_HTT66	1 66 Mhz 3.3V single ended HTT clock
SEL_SATA	0* 100 Mhz differential HTT clock
SEL_27	1 100 Mhz non-spreading differential SRC clock
	0* 100 Mhz spreading differential SRC clock
	1* 27Mhz non-spreading singled clock
	0 100 Mhz spreading differential SRC clock



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

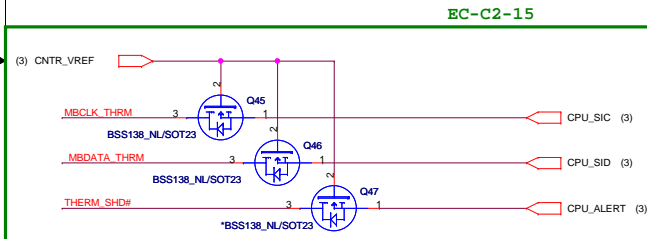
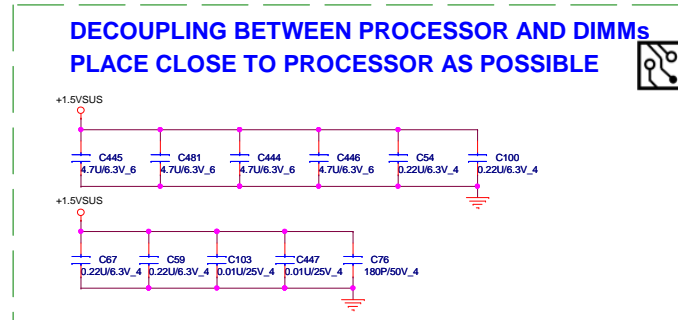
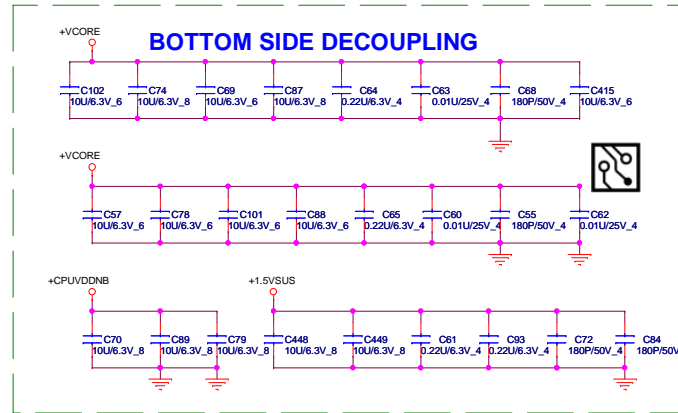
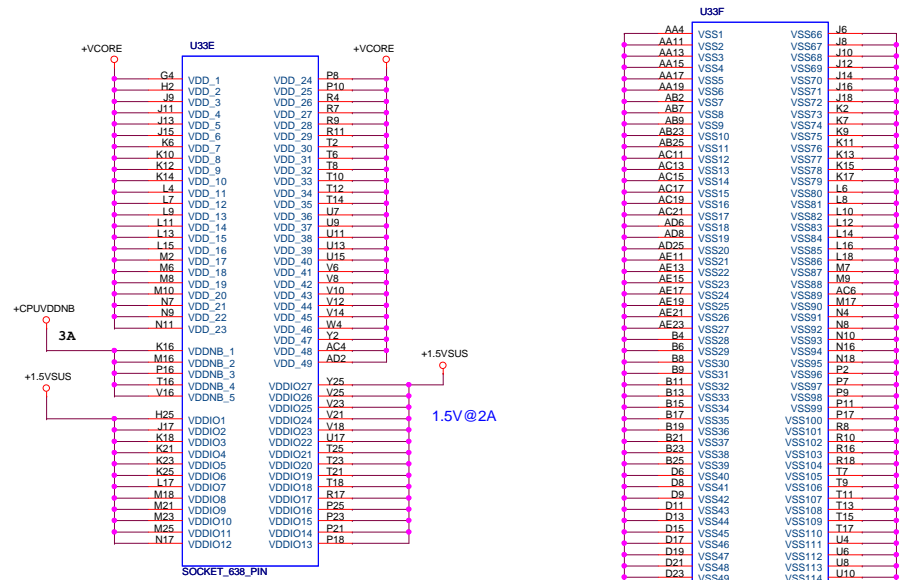




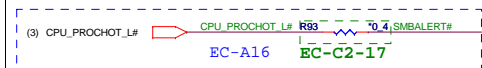
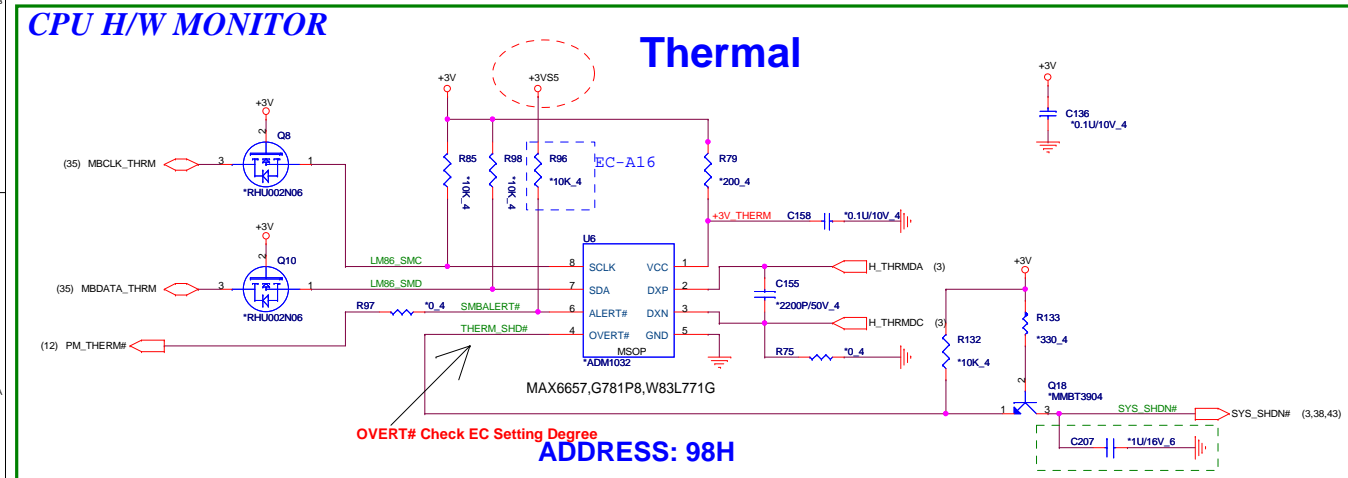
PROCESSOR POWER AND GROUND

(42,43) +VCORE
(42,43) +CPUVDDNB
(3,4,15,16,39,41,42,43) +1.5VSUS
(2,3,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,28,30,31,34,35,40,41,43) +3V

05



EC-C2-20





Close to NB within 1'

This block is for UMA only , Discrete can remove all component



IOPLLVDD18 - memory PLL
not applicable to RX881

IOPLLVD- memory PLL
not applicable to RX881

Add RST# connection to SB800 F

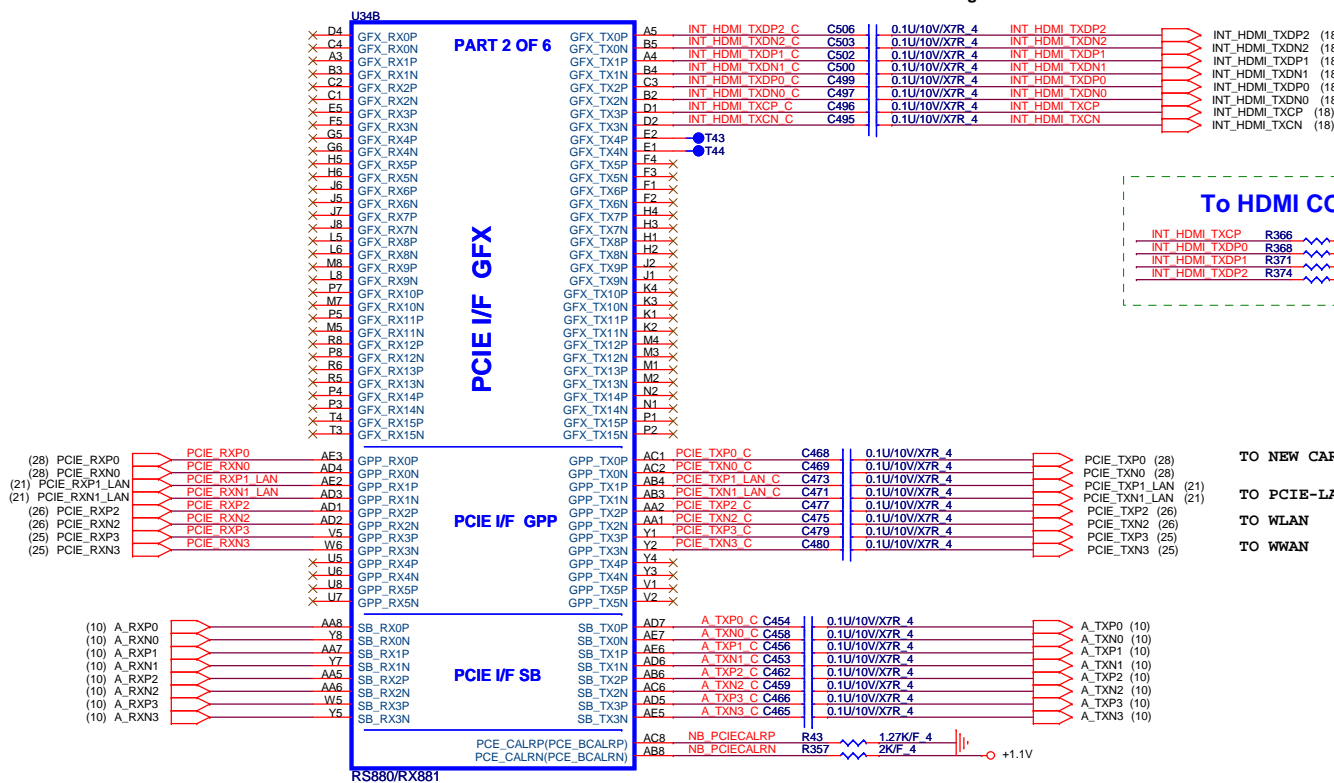
R81 is only for power consumption
Customer should connect MEM_VDDQ directly to a plane

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

(2,3,6,8,9,13,40,43) +1.1V

Close to North Bridge



EC-C-27

To HDMI CONN

INT_HDMI_TXCP R366 *80.6/F 4 INT_HDMI_TXCN
 INT_HDMI_TXDP0 R368 *80.6/F 4 INT_HDMI_TXDN0
 INT_HDMI_TXDP1 R371 *80.6/F 4 INT_HDMI_TXDN1
 INT_HDMI_TXDP2 R374 *80.6/F 4 INT_HDMI_TXDN2

TO NEW CARD

TO PCIE-LAN

TO WLAN

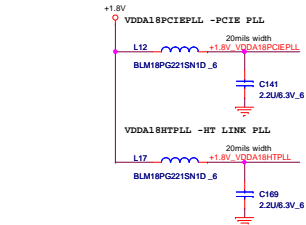
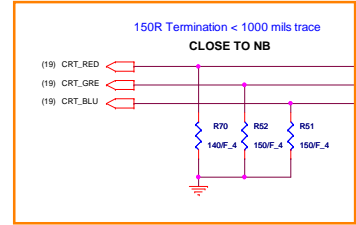
TO WWAN



Quanta Computer Inc.

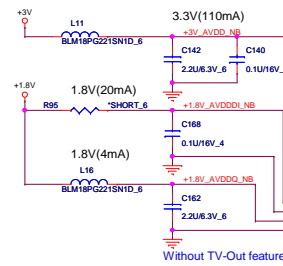
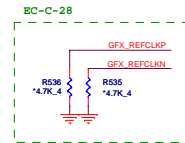
PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A
Date:	Thursday, April 01, 2010	Sheet 7 of 49

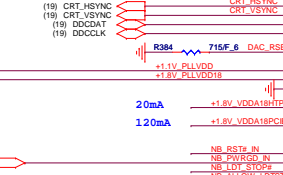


North Bridge A-Link

20091022



Without TV-Out feature



20091022 HT NB

(2) CLK_NB_HTTREPP
(2) CLK_NB_HTTREFF

(2) CLK_SBLINKP
(2) CLK_SBLINKN

(2) EXT_NB_OSC

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

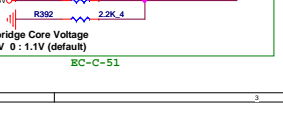
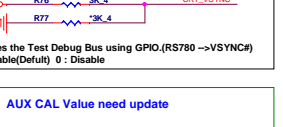
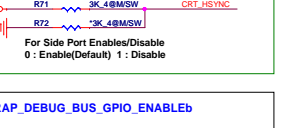
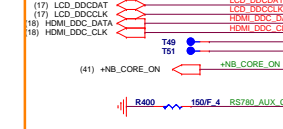
(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN

(2) CLK_NB_GFXP
(2) CLK_NB_GFXN



PART 3 OF 6

CRT/VOUT

PM PLL PWR

LVTM

CLOCKS

MIS.

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

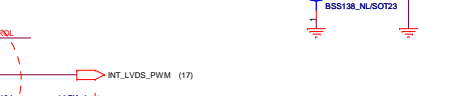
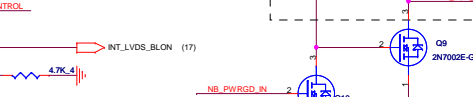
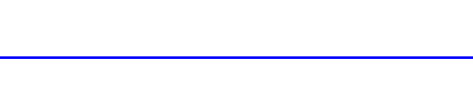
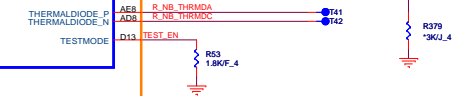
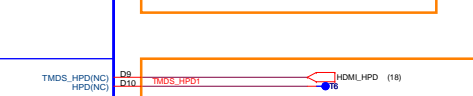
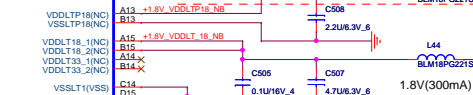
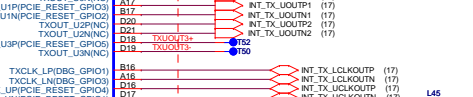
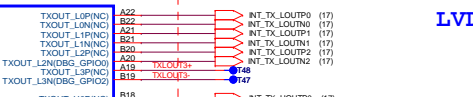
LVDS

LVDS

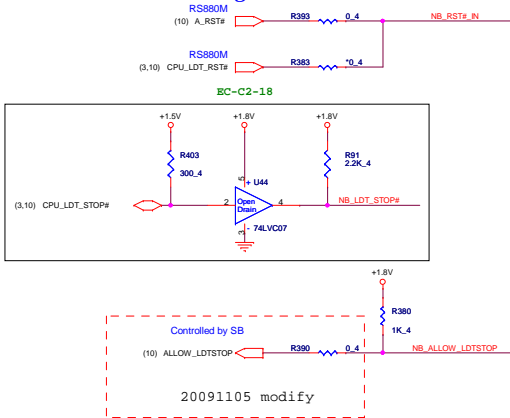
LVDS

LVDS

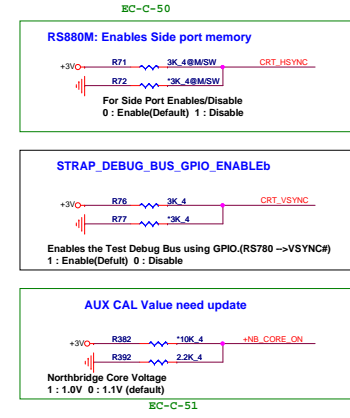
LVDS



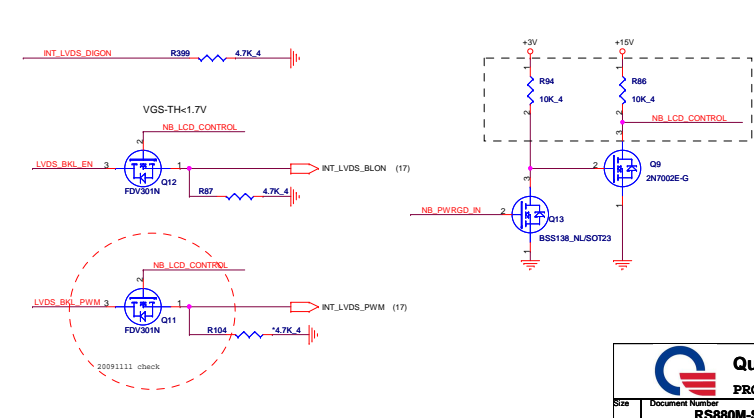
North Bridge RESET



STRAP DEBUG BUS GPIO



LVDS BLON

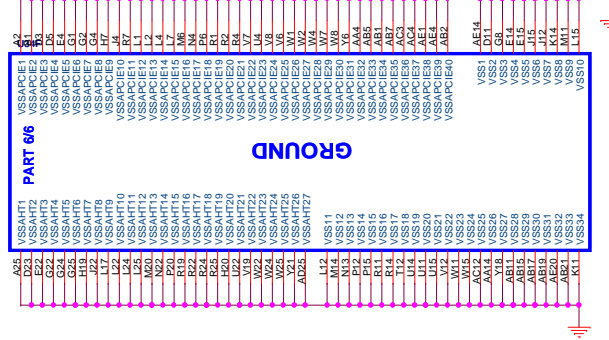


RX881/RS880 POWER DIFFERENCE TABLE

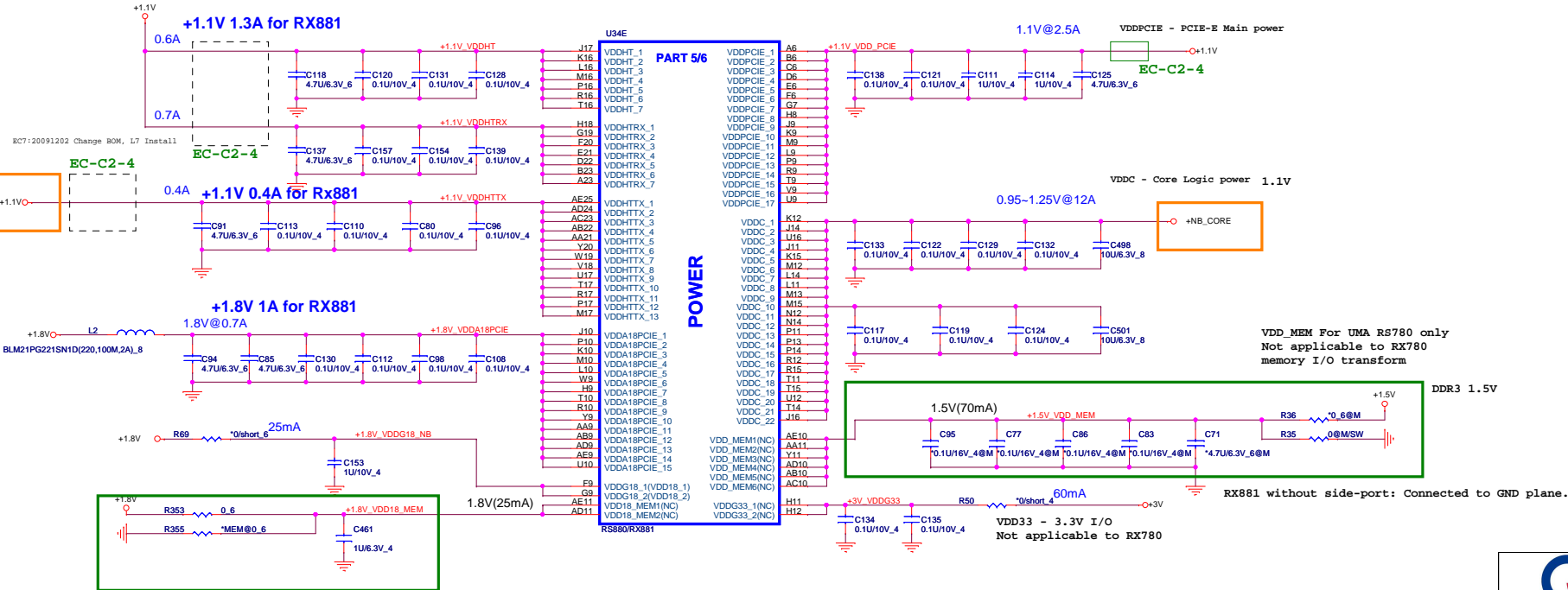
PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVD0	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD0	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVD018	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLTP18	GND	+1.8V
IOPLLVD018	+1.8V	+1.8V	VDDLTP33	NC	NC

(2,3,5,8,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,28,30,31,34,35,40,41,43)

(41,43) +NB_CORE
(2,3,6,7,8,13,40,43) +1.1V
(3,6,25,26,28,43) +1.5V
(6,8,14,40,43) +1.8V
+3V



GROUND



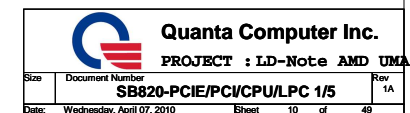
POWER



Quanta Computer Inc.

PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	RS880M-POWER5 4/4	1A
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SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

SATA ODD

E-SATA

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

EC-C-30

U38B

SB800
Part 2 of 5

FLASH

SERIAL ATA

HW MONITOR

SPI ROM

SB800 A11

(5,10,11,13,14,23,26,43) +3VS5
(2,3,5,8,9,10,11,13,14,15,16,17,18,19,20,21,22,23,24,25,26,28,30,31,34,35,40,41,43) +3V

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

3.3v(5v-tolerance)

checklist

EC-C-52 EC-C2-1

+3VS5

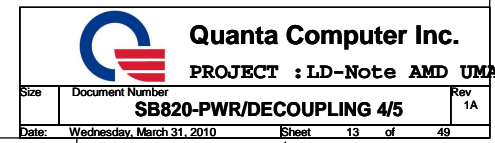
ID3	ID2	ID1	ID0	
0	X	X	X	LD GC5C UMA(14")
1	X	X	X	LD GC6C UMA(15")
X	0	0	0	SDV
X	0	0	1	SIT
X	0	1	0	SIT-R
X	0	1	1	SVT
X	1	0	0	SOVP



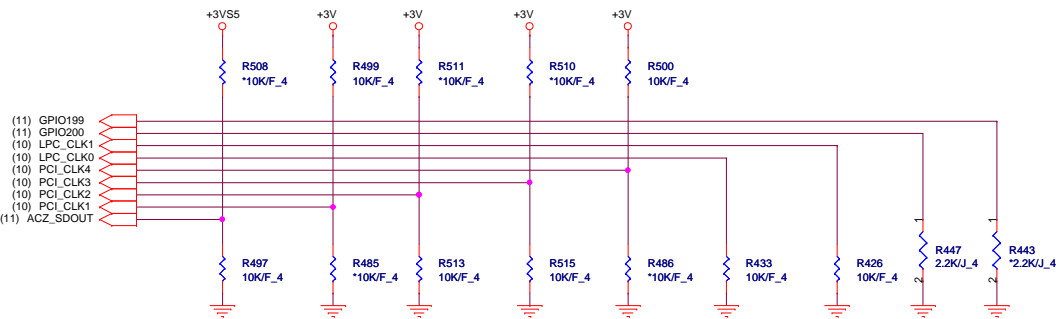
Quanta Computer Inc.

PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	SB820-SATA/IDE/HWM/SPI 3/5	1A
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REQUIRED STRAPS



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L, H=LPC ROM DEFAULT L, L=FWH ROM	

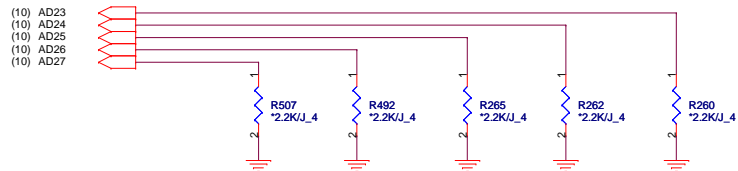
internal have
pull Hi 10K



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

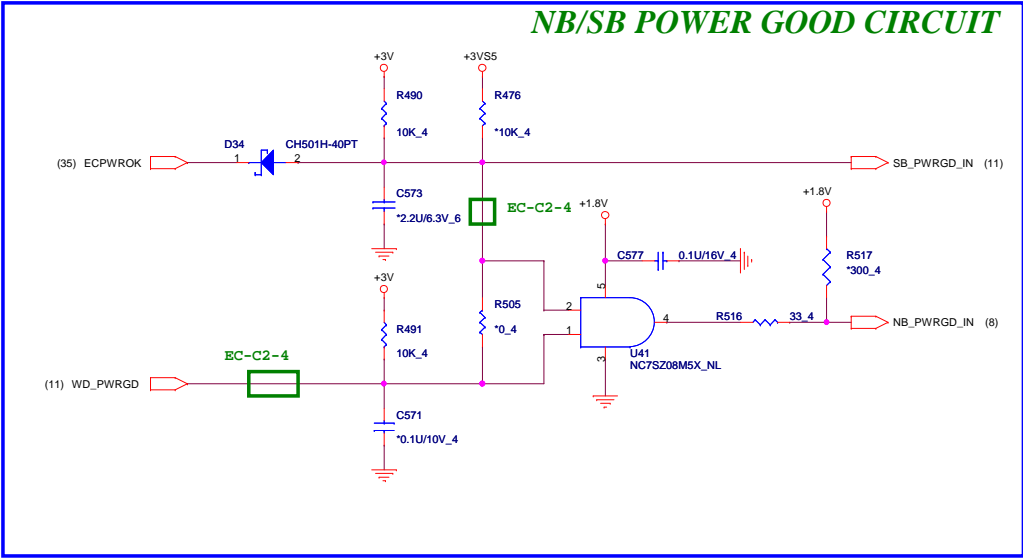
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



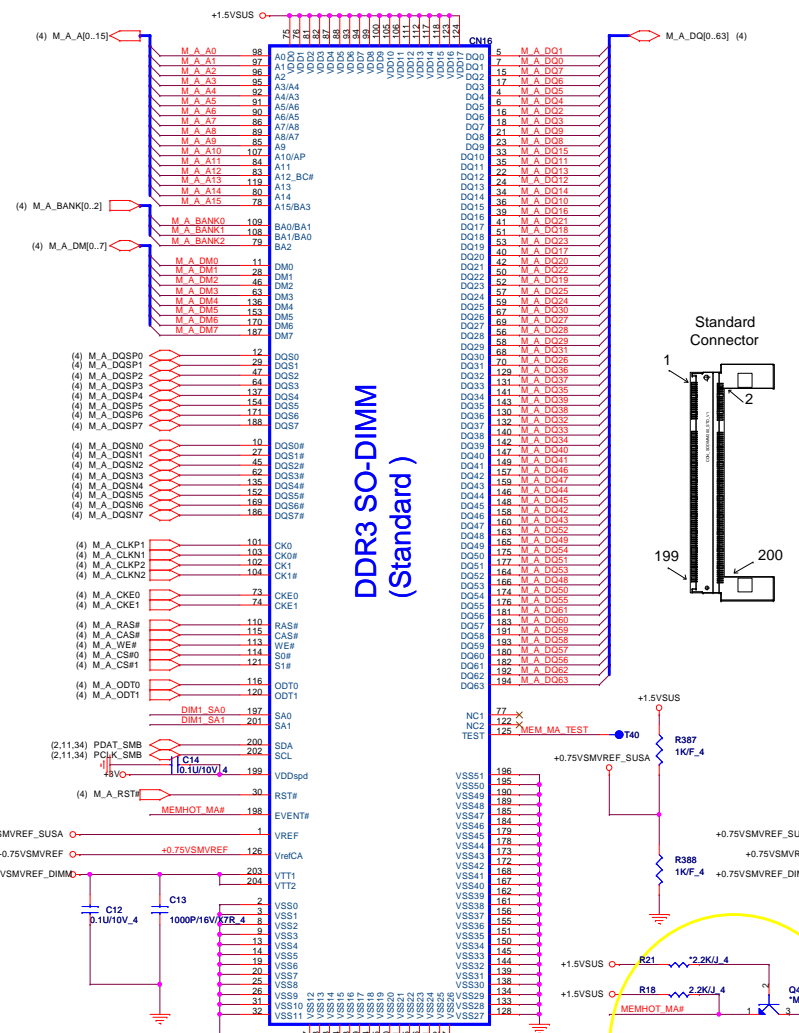
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

Place these Caps near So-Dimm0.

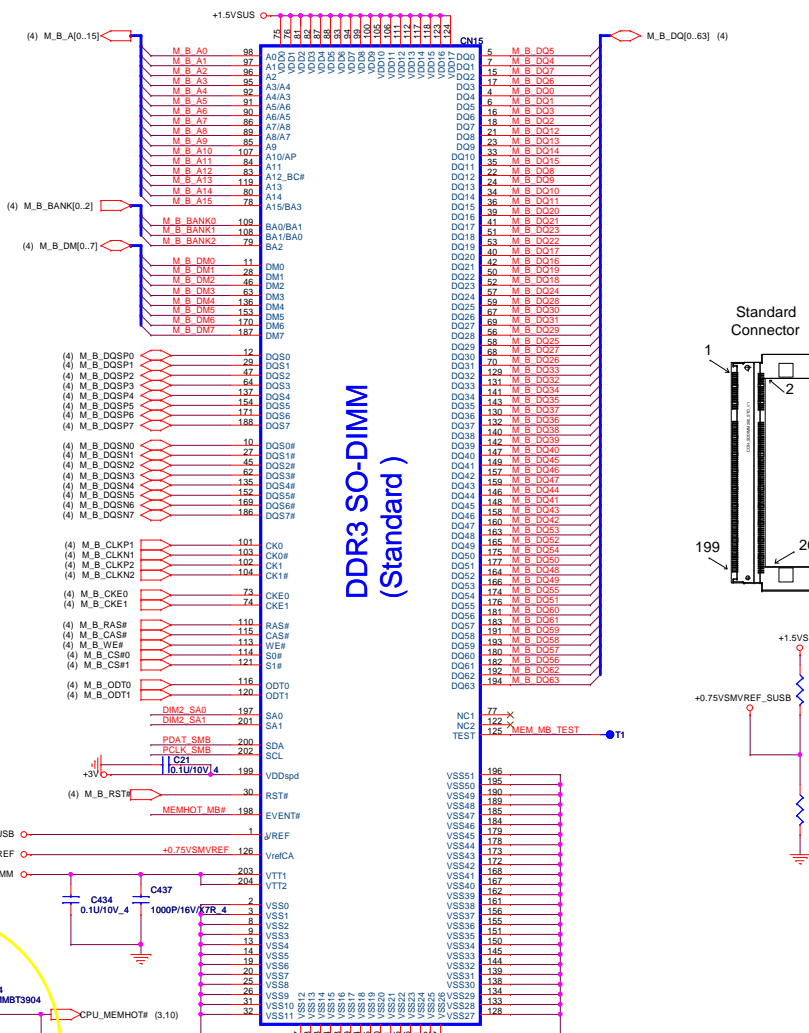
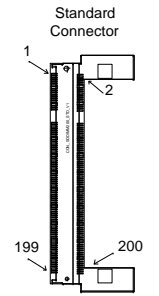
Place these Caps near So-Dimm1.

(4,16,38) +0.75VSMVREF
(3,4,5,16,38,41,42,43) +1.5VSUS
(16,38,43) +0.75VSMVREF_DIMM
(2,3,5,8,9,10,11,12,13,14,16,17,18,19,20,21,22,23,24,25,26,28,30,31,34,35,40,41,43) +3V

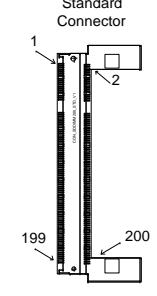
15



DDR3 SO-DIMM
(Standard)



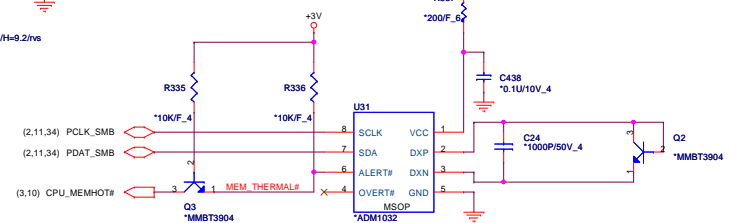
DDR3 SO-DIMM
(Standard)



(DIMM-0 H=5.2)

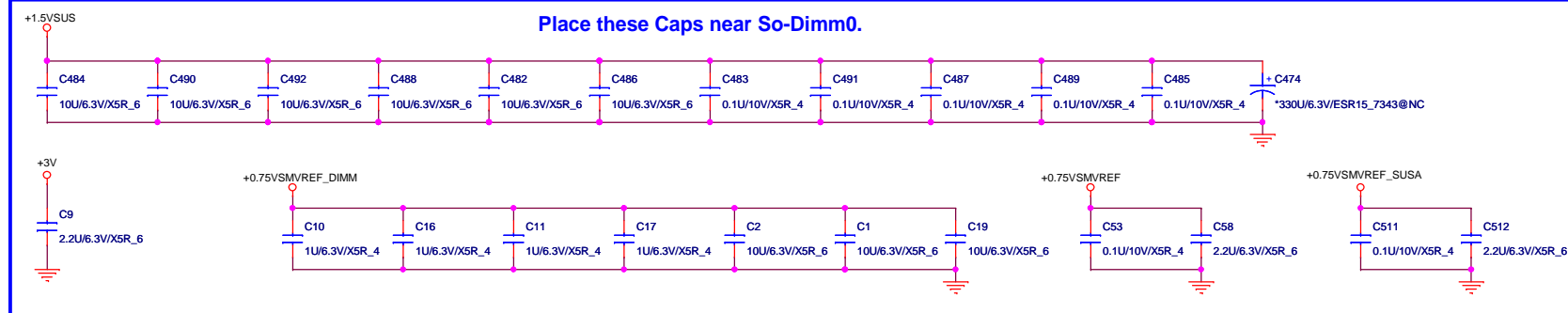
(DIMM-1 H=9.2)

DDR3-DIMM1/H=9.2/2vs

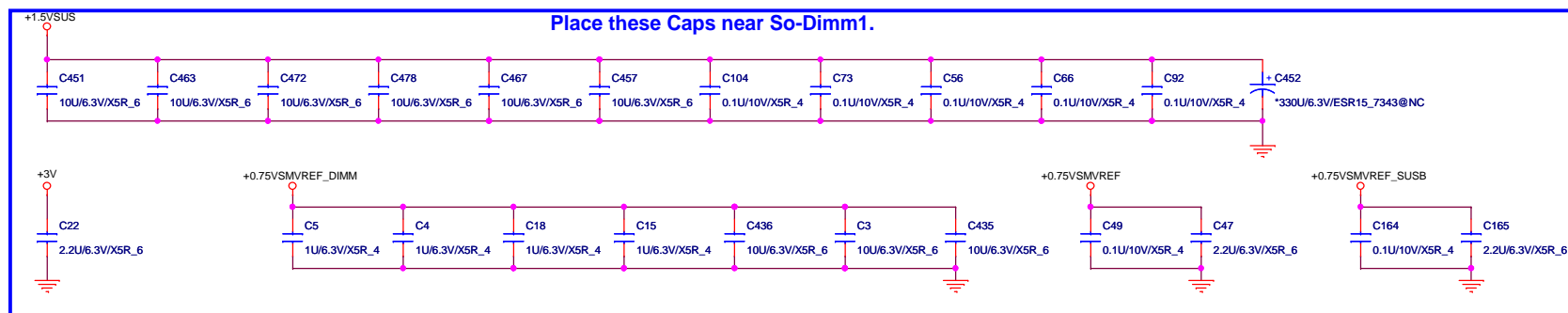


Close DDR3 socket

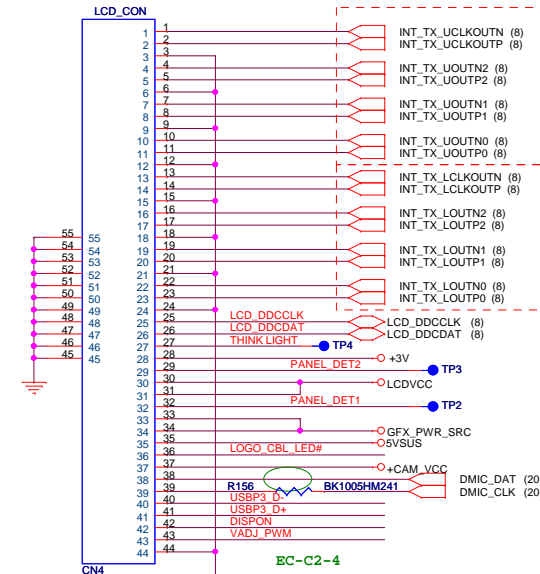
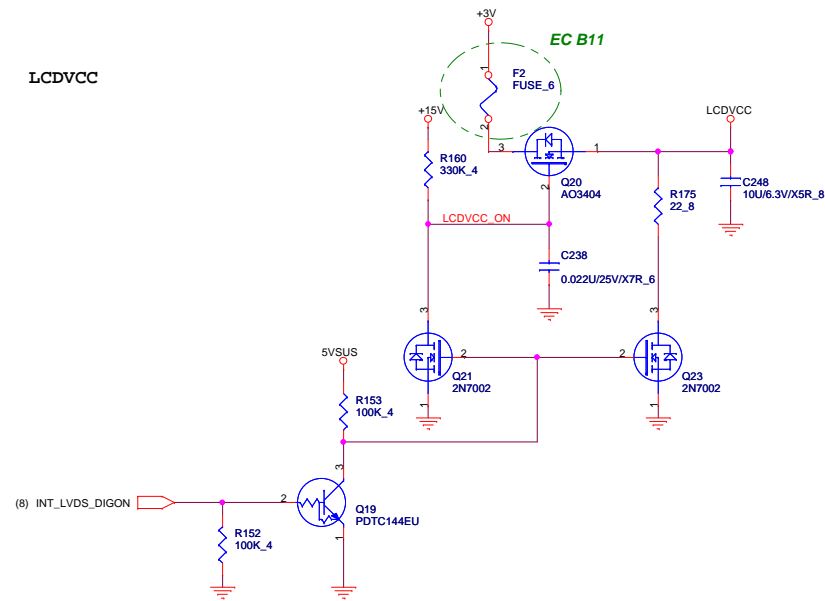
Place these Caps near So-Dimm0.



Place these Caps near So-Dimm1.

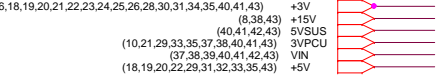


LCDVCC



Address : A9H --Contrast
AAH --Backlight

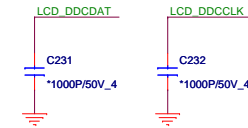
(2,3,5,8,9,10,11,12,13,14,15,16,18,19,20,21,22,23,24,25,26,28,30,31,34,35,40,41,43)



17

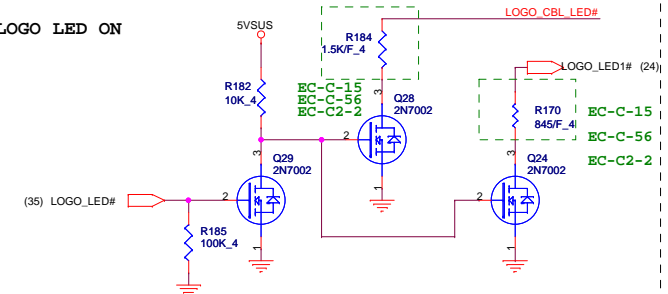


For EMI

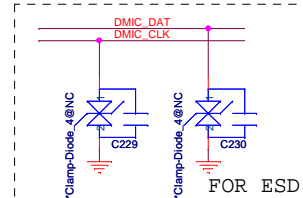
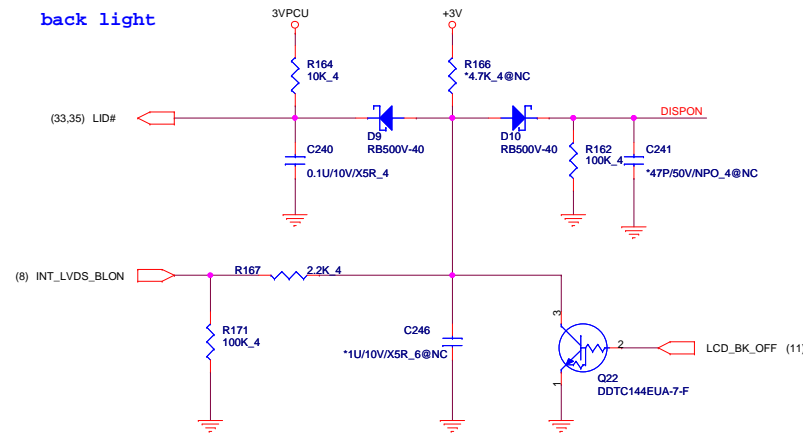


20091229 change BOM R184,R170

LOGO LED ON

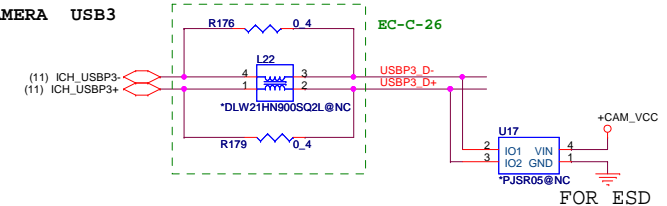


back light

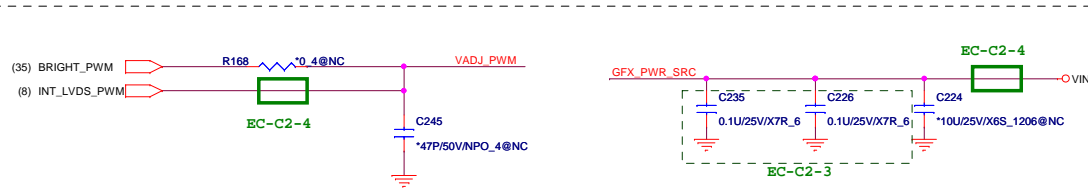
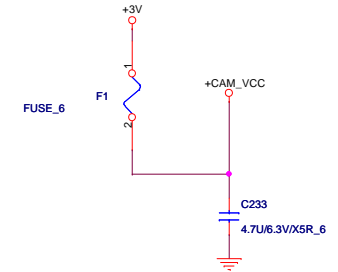


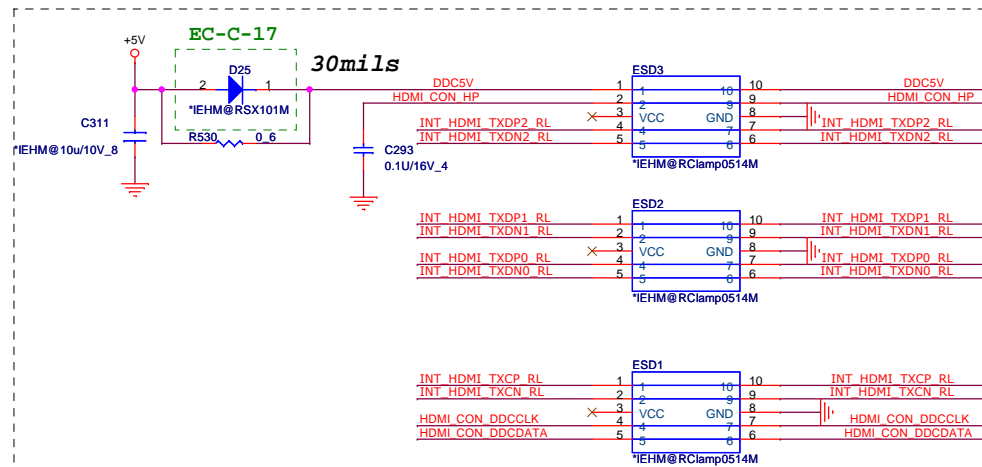
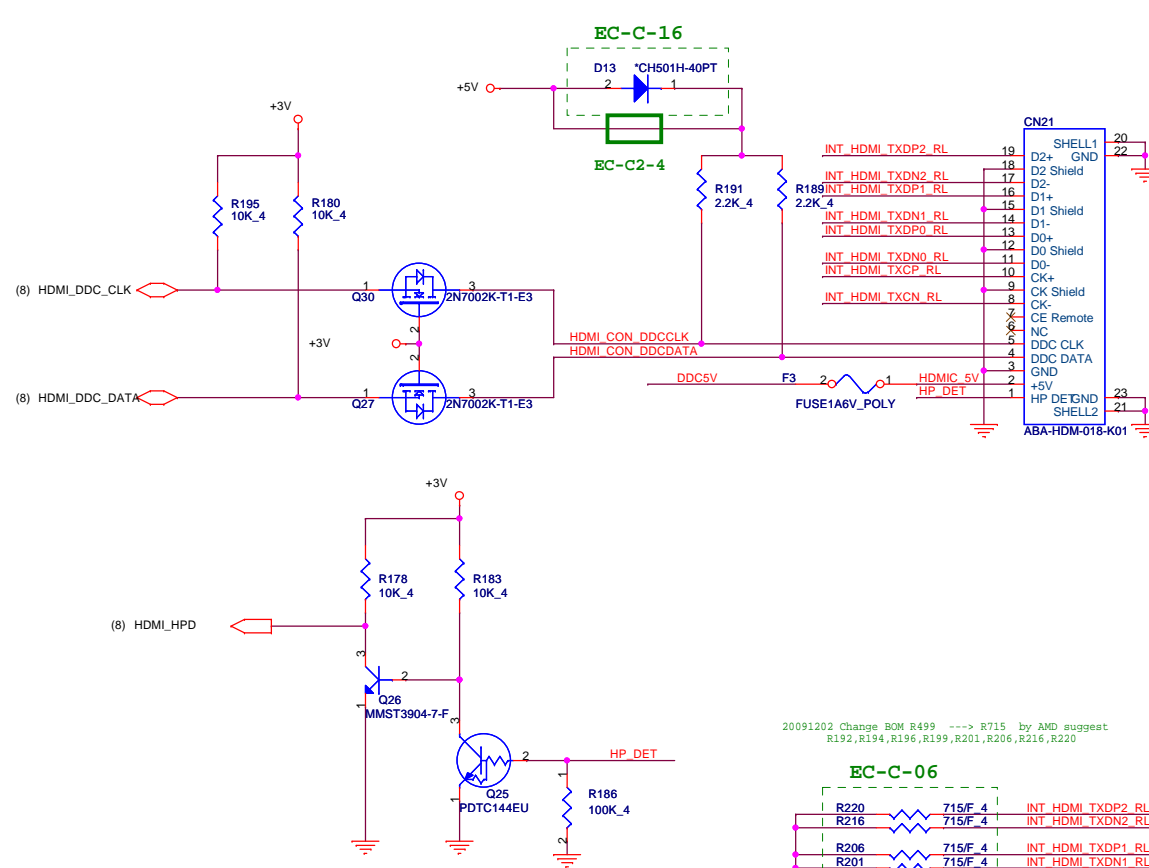
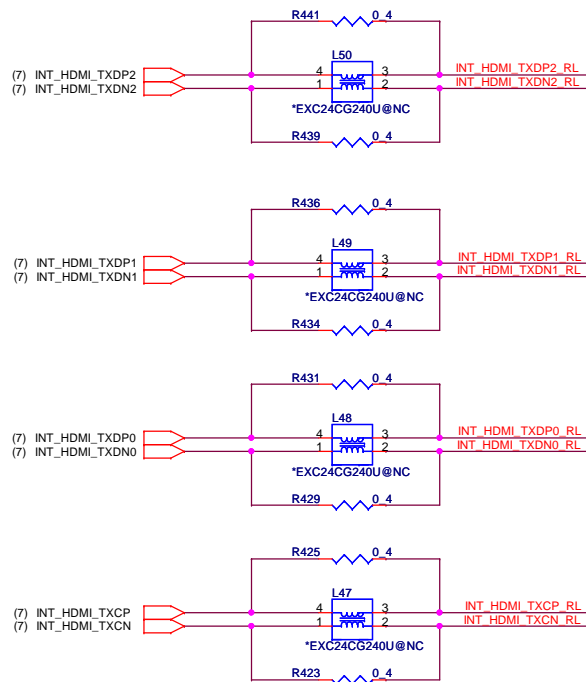
FOR ESD

CAMERA USB3



CAMERA VCC Control

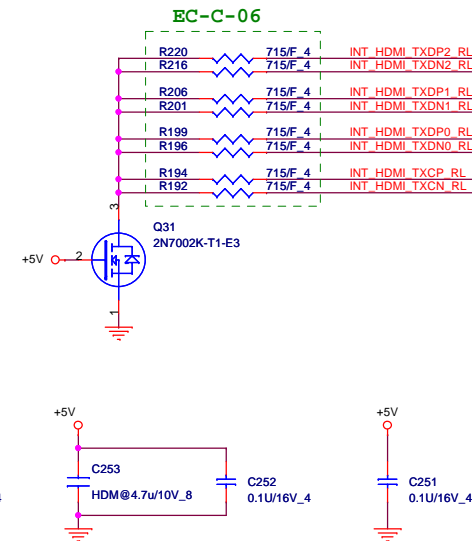




For ESD

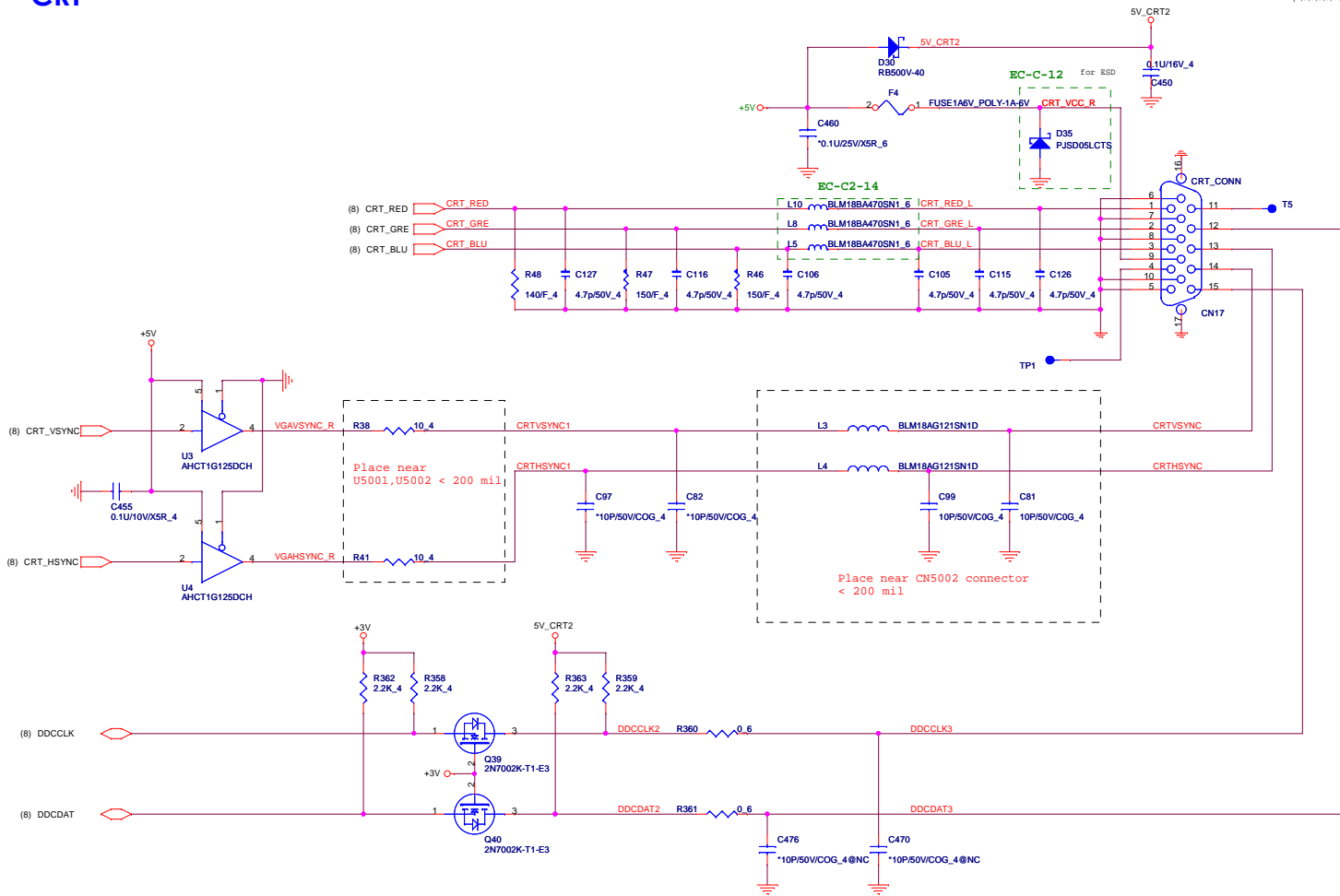
Layout note: Place close to HDMI Conn

20091202 Change BOM R499 ----> R715 by AMD suggest
R192, R194, R196, R199, R201, R206, R216, R220

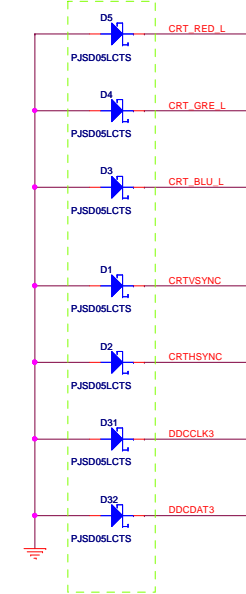


Quanta Computer Inc.

PROJECT : LD-Note AMD UMA

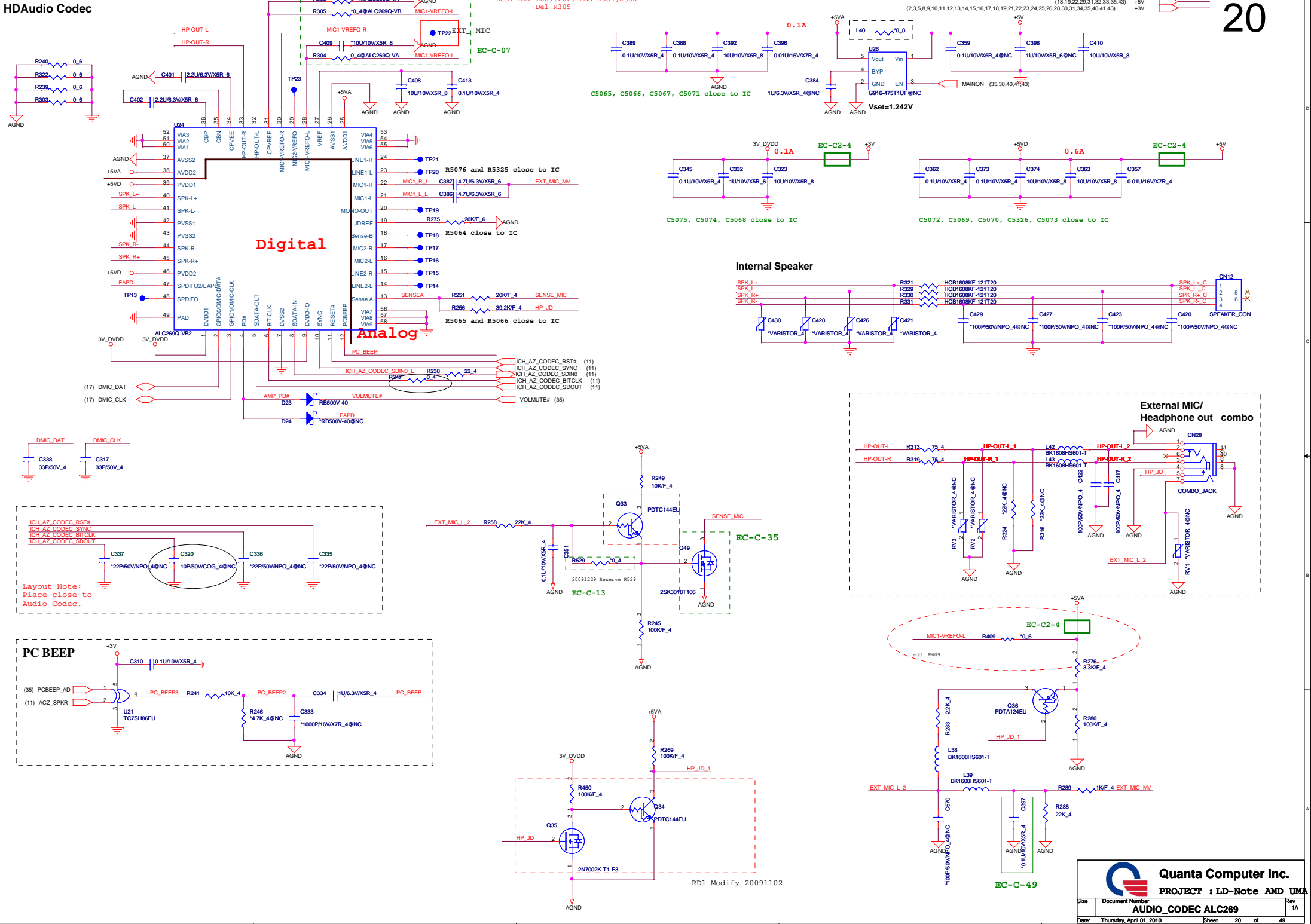


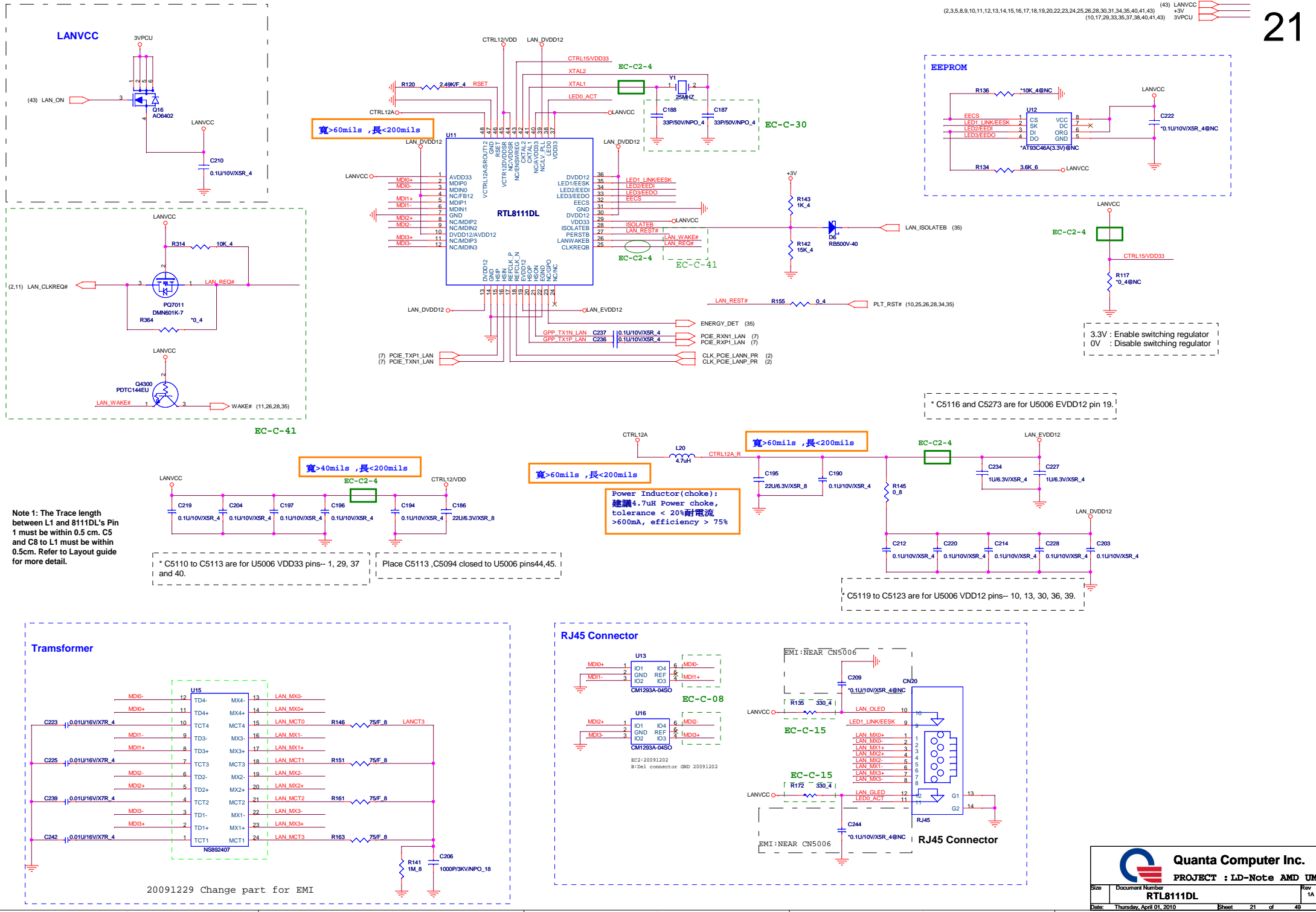
ESD PROTECTION



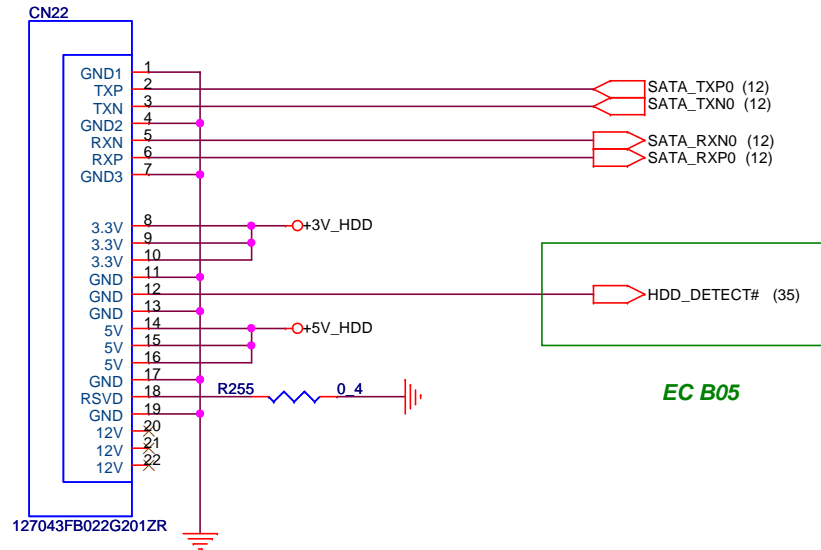
HDAudio Codec

20





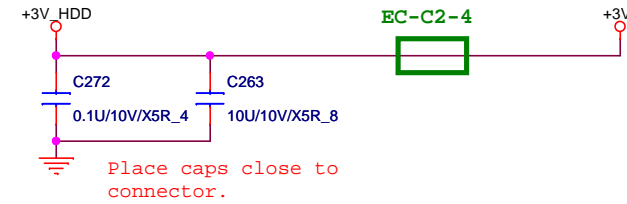
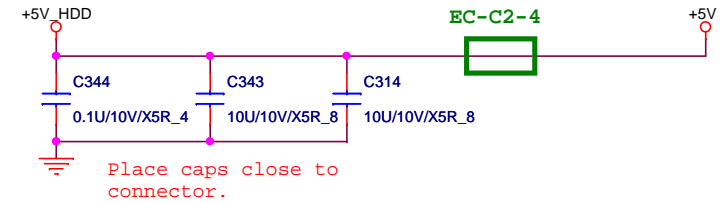
SATA HDD Connector.



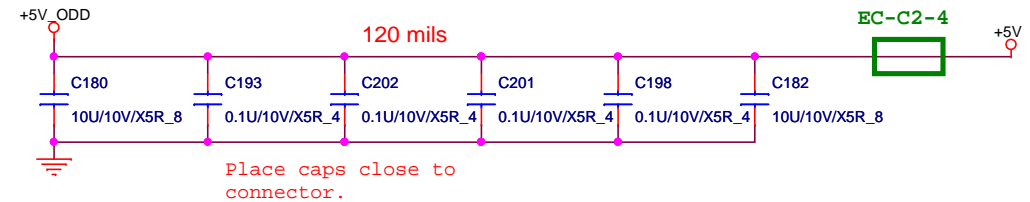
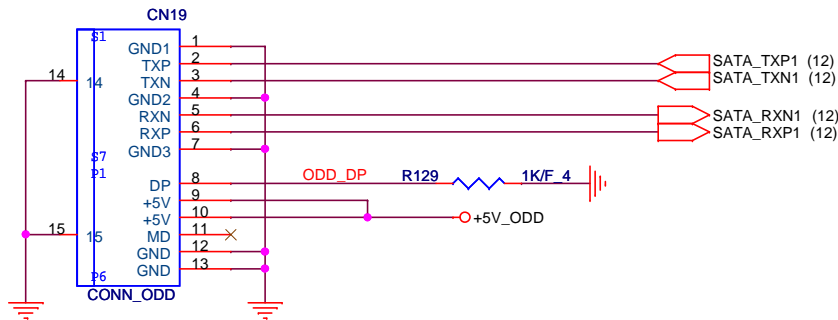
(18,19,20,29,31,32,33,35,43) +5V
(2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,23,24,25,26,28,30,31,34,35,40,41,43) +3V



22



ODD Connector



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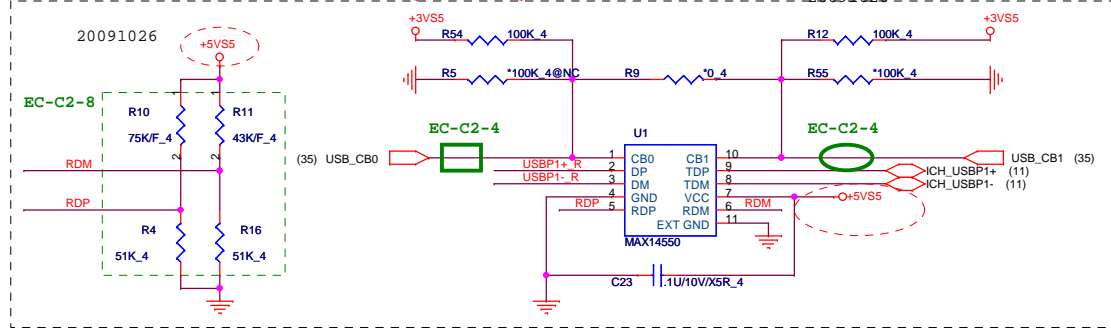
PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	1A
Date:	Wednesday, March 31, 2010	Sheet 22 of 49

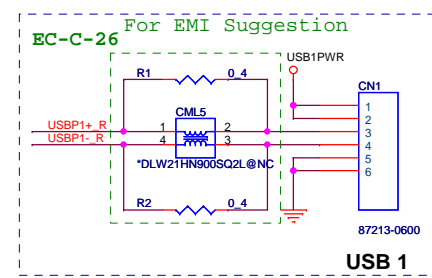
USBX1

23

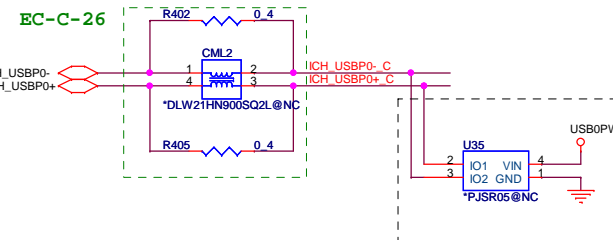
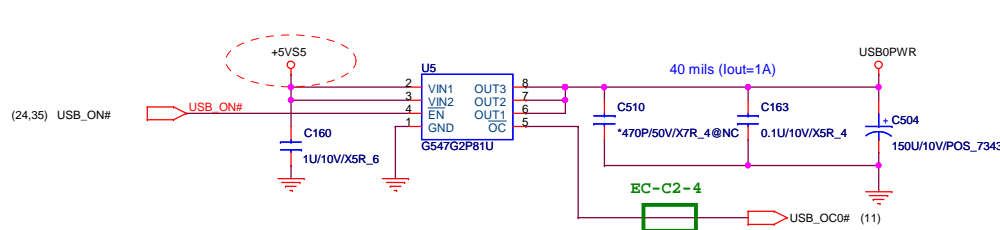
Support Black-berry function



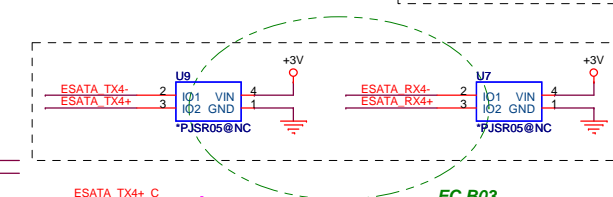
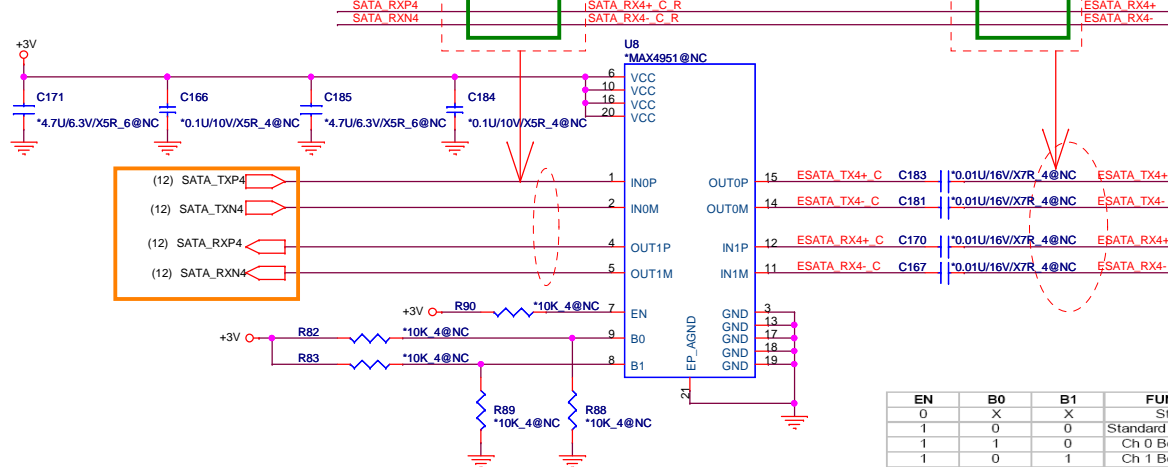
USB X1---> Wire to board conn



USB + E-SATA



E-SATA RE-DRIVER



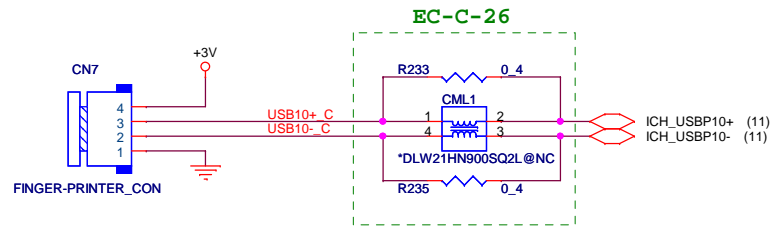
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



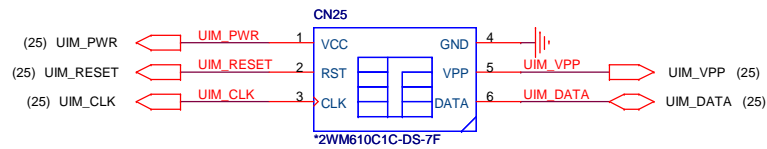
Quanta Computer Inc.

PROJECT :LD-Note AMD UMA

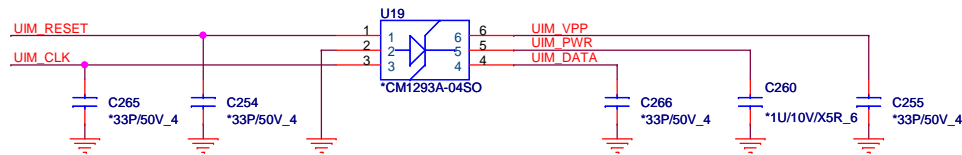
Finger Print



SIM Card CONN



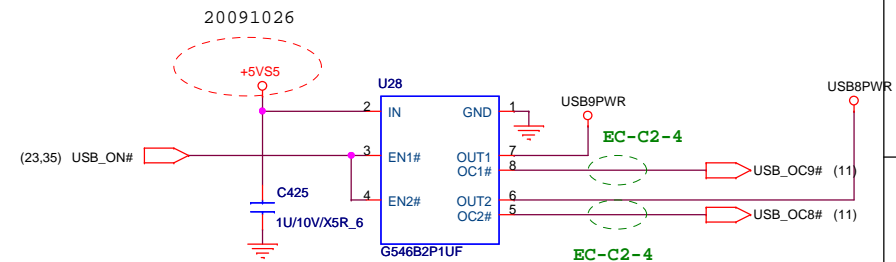
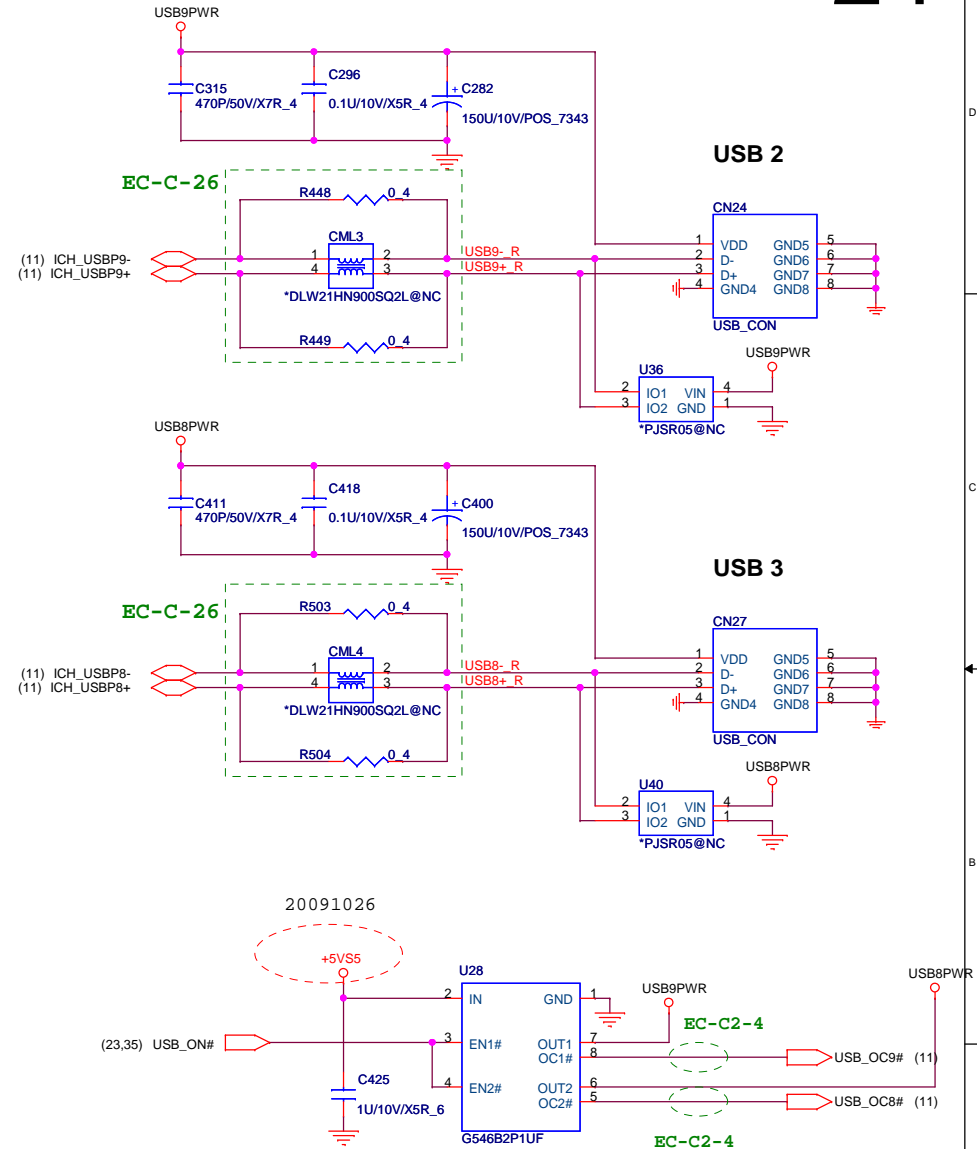
Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible



FRONT LEDs



20091229 del R268 221/F 4



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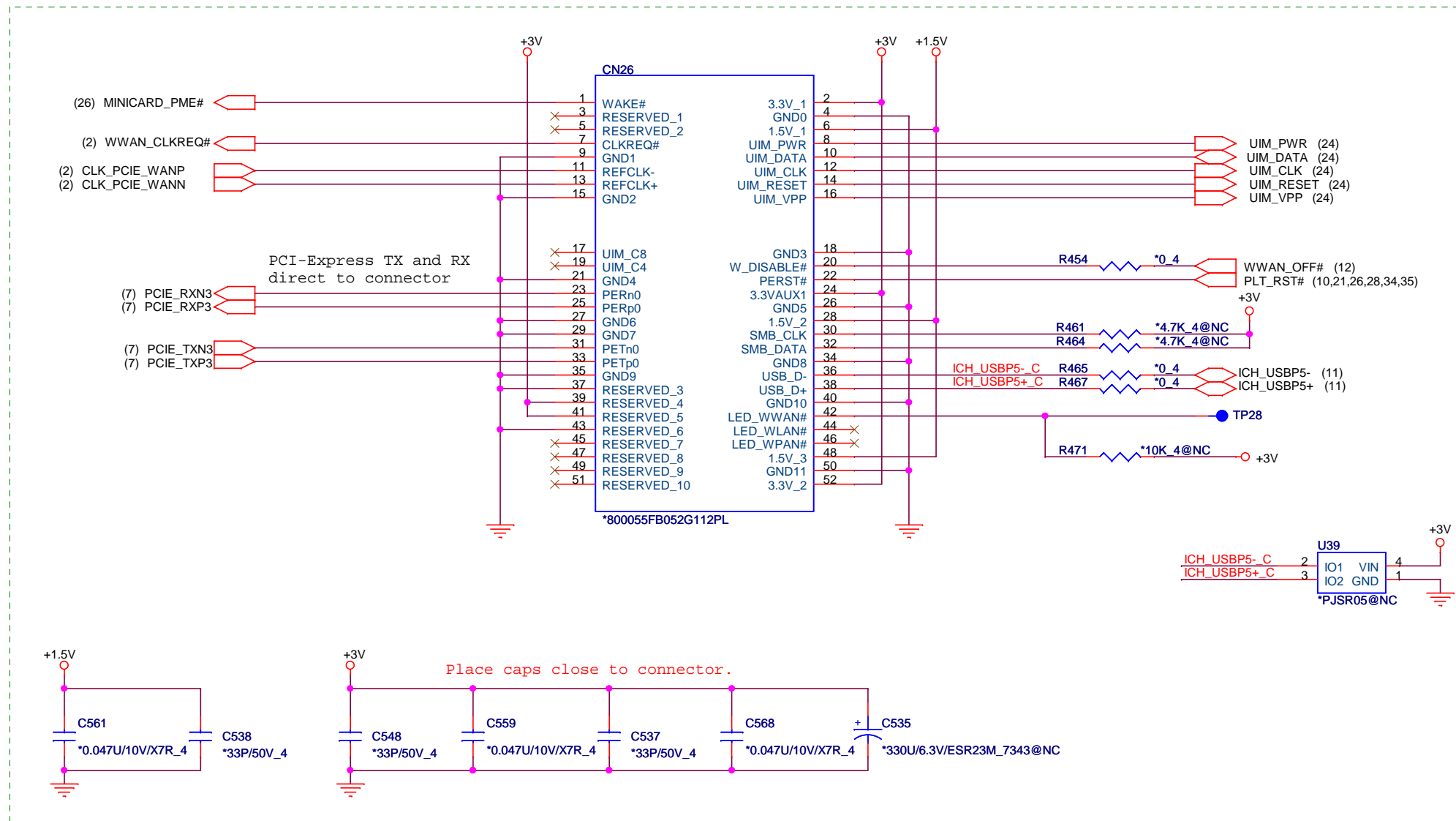
PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	USB X2/SIM_CARD/LEDs/RF	1A
Date:	Wednesday, March 31, 2010	Sheet 24 of 49

MiniCard WWAN connector

EC-C-53

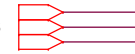
25



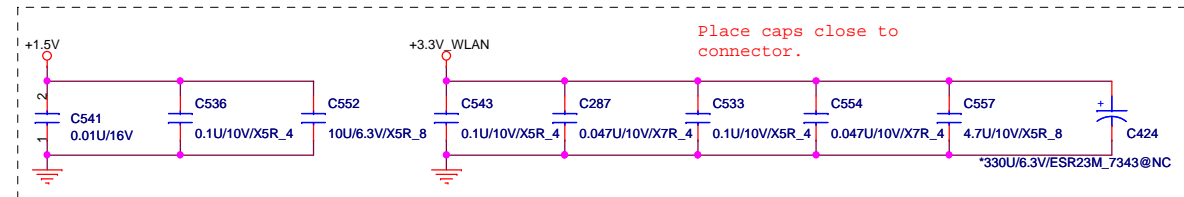
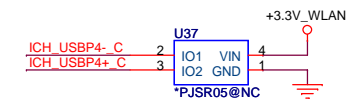
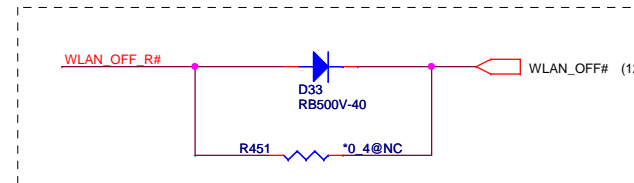
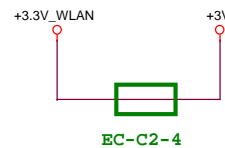
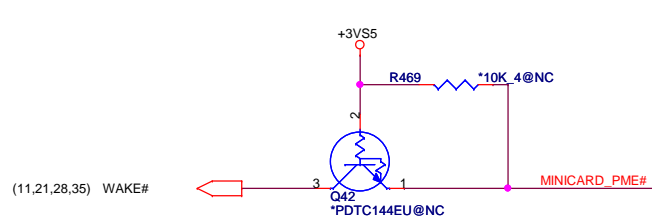
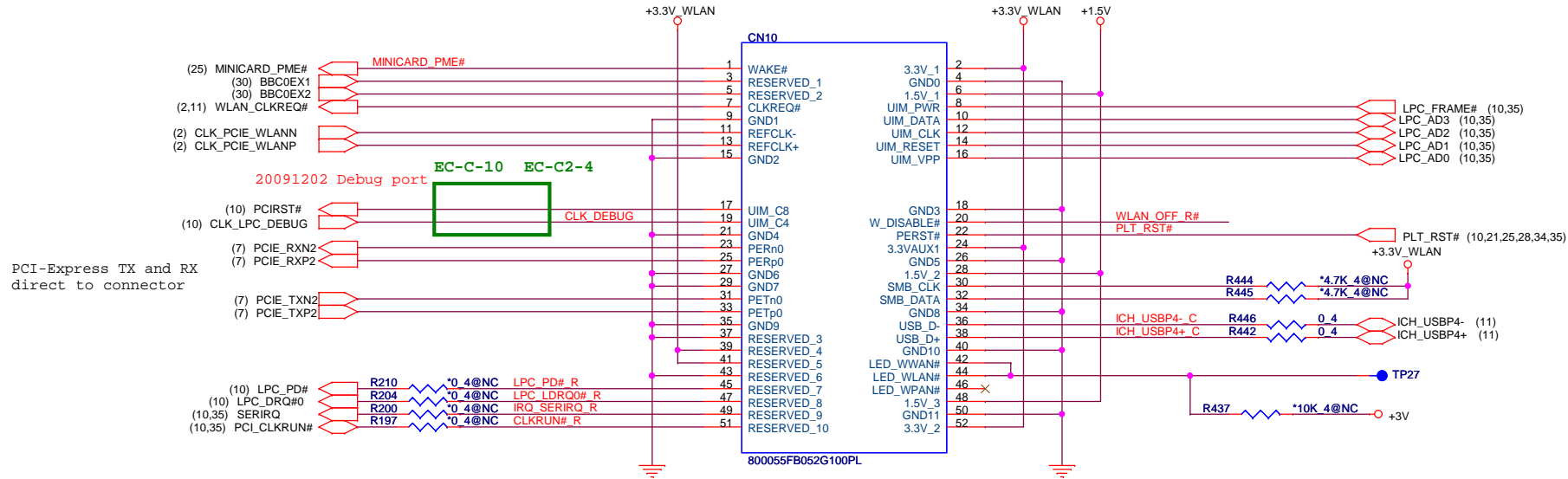
MiniCard WLAN/WiMAX connector

(2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,28,30,31,34,35,40,41,43)

+3V
(5,10,11,12,13,14,23,43)
+3VS5
(3,6,9,25,28,43)
+1.5V



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PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	MINI-Card (WLAN)	1A
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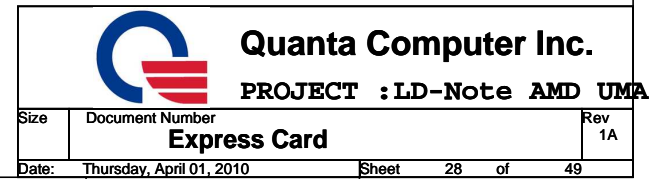
	SD/MMC	MS	XD
SP0			
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4			XD D4
SP5		MS BS	XD D5
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		
SP13	SD DAT4		XD WP#
SP14			XD R/B#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

[illegible]

0616 Add 10K to GND for +3VCARD discharge in Ver.B

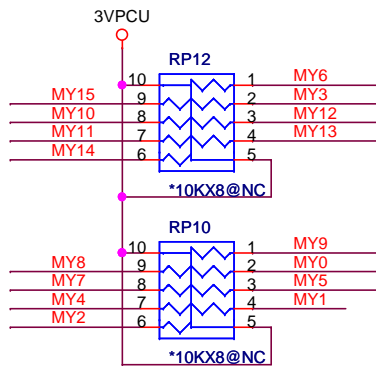
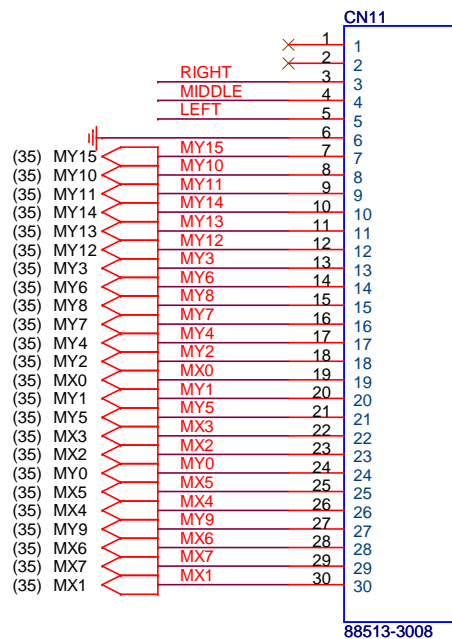
0505 EMI added

28



KEYBOARD

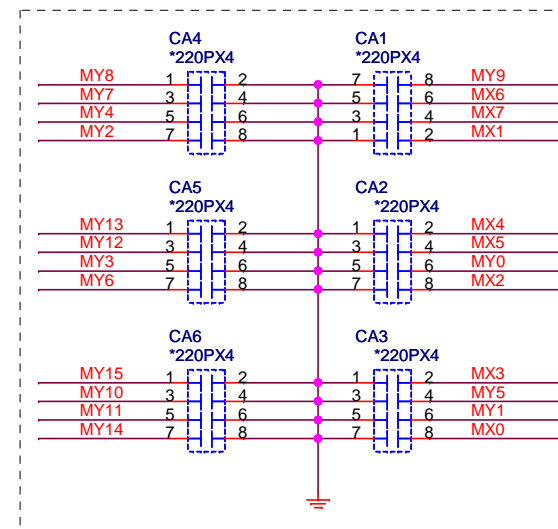
KEYBOARD connector



(18,19,20,22,31,32,33,35,43) +5V
(10,17,21,33,35,37,38,40,41,43) 3VPCU

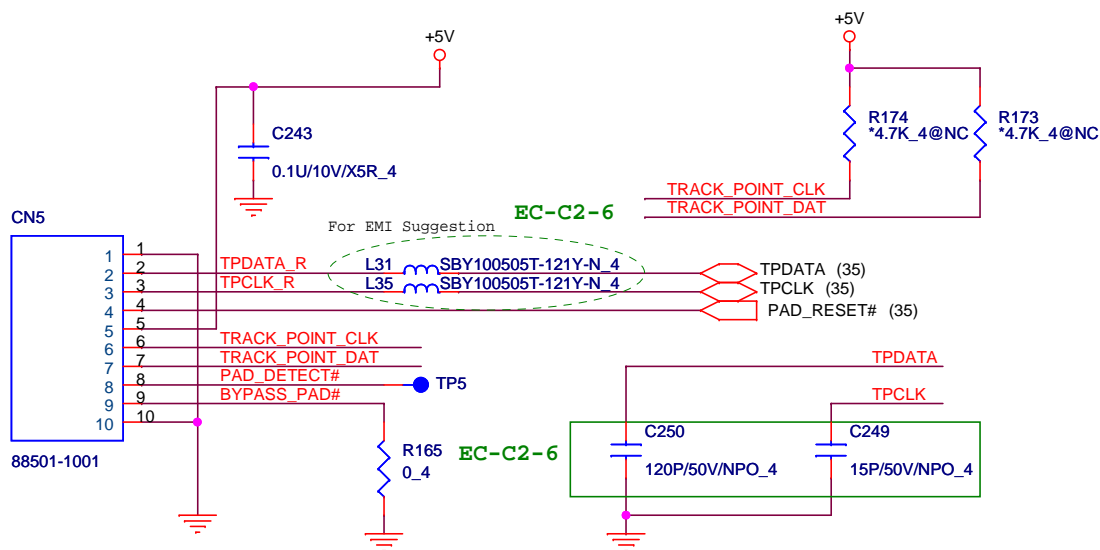


29

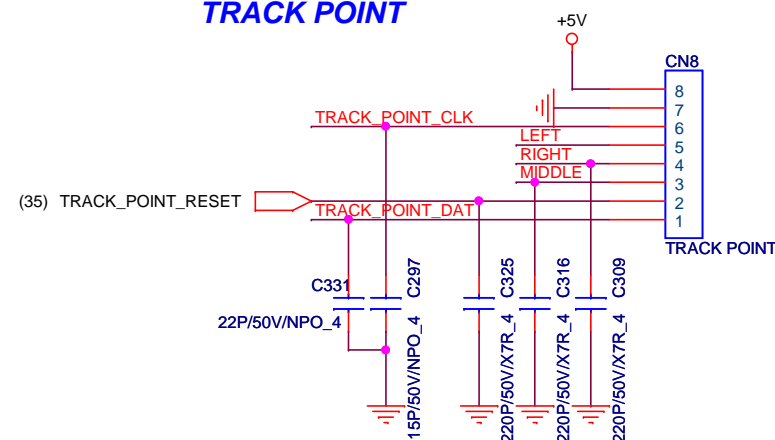



For EMI request

Touch pad



TRACK POINT





Quanta Computer Inc.
PROJECT :LD-Note AMD UMA

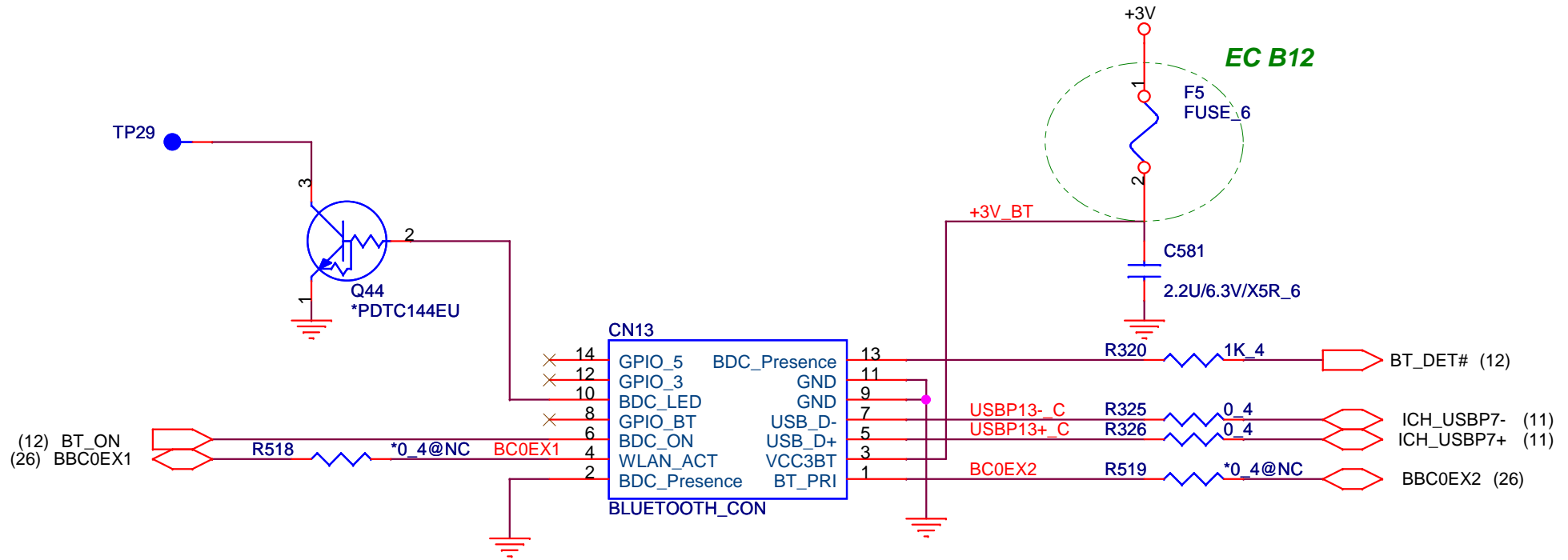
Size	Document Number	Rev
	K/B, T/P	1A
Date:	Wednesday, March 31, 2010	Sheet 29 of 49

BLUETOOTH

(2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,28,31,34,35,40,41,43)

+3V

30

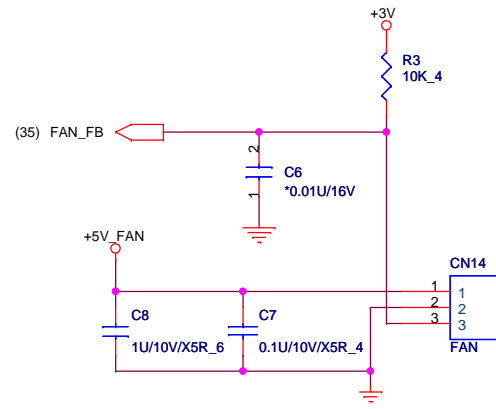
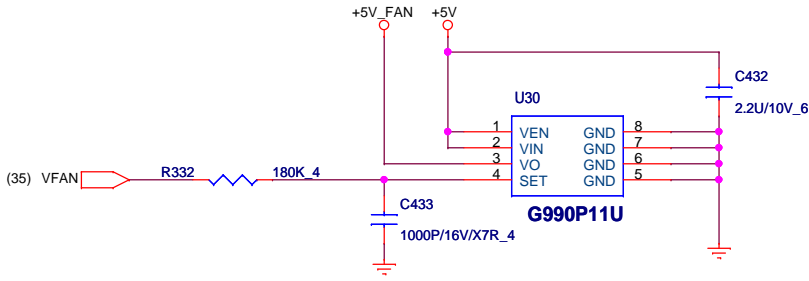


Quanta Computer Inc.

PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	B/T	1A
Date:	Thursday, April 01, 2010	Sheet 30 of 49

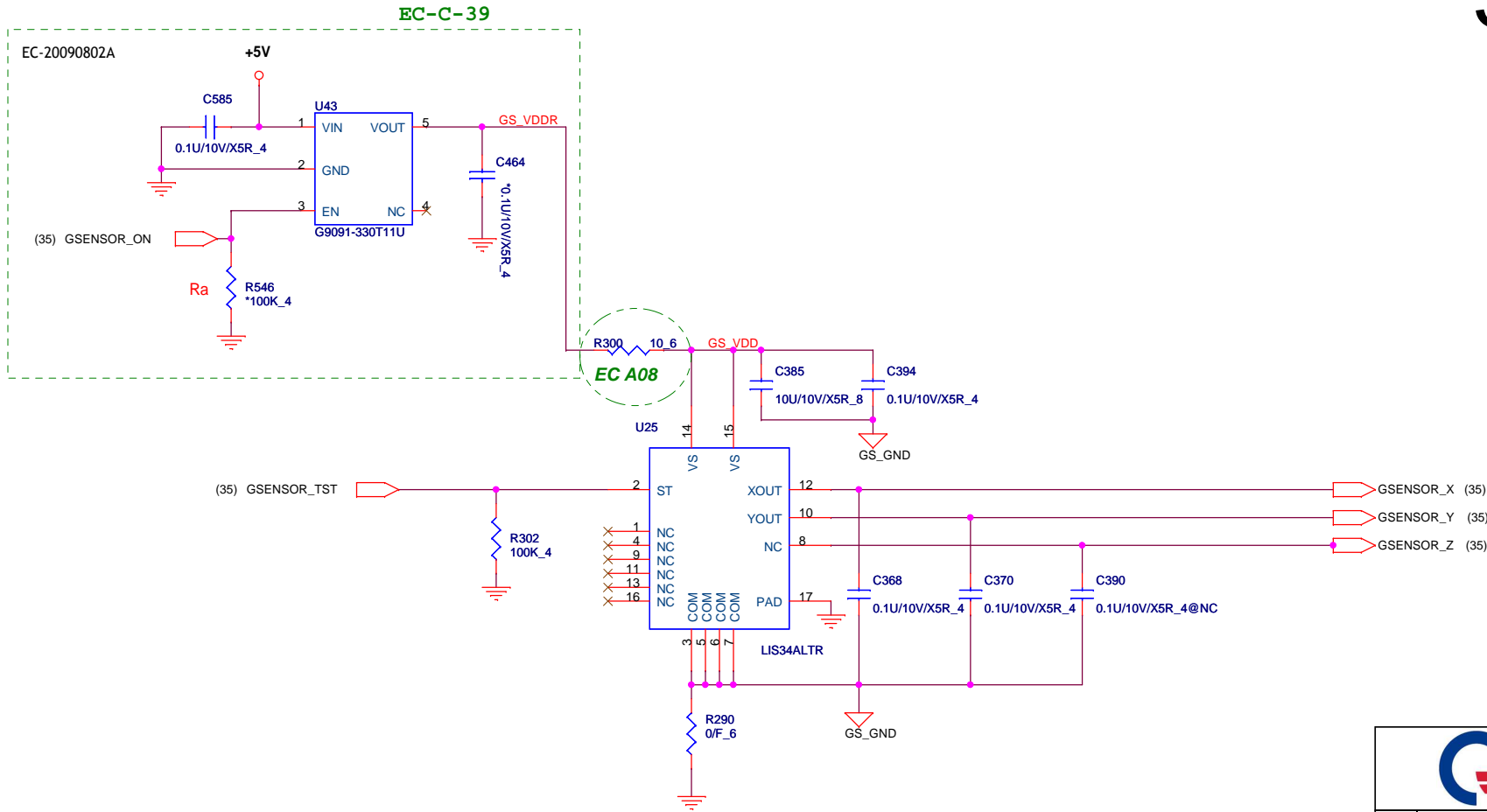
FAN CONTROL




G-SENSOR (3-Axial)

(2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,28,30,31,34,35,40,41,43)
+3V
(8,17,38,43) +15V

32





Quanta Computer Inc.

PROJECT : LD-Note AMD UMA

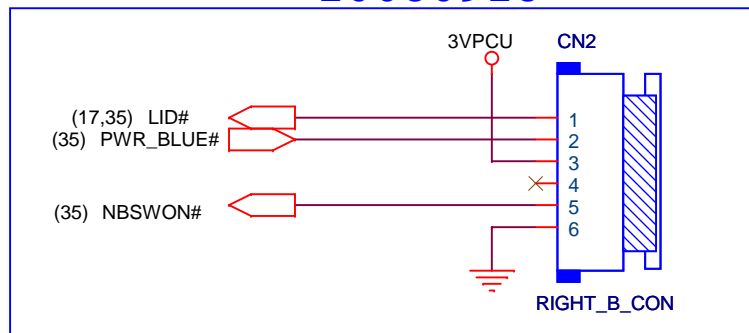
Size	Document Number	Rev
	G-SENSOR	1A
Date:	Wednesday, March 31, 2010	Sheet 32 of 49

FFC TO B LED RIGHT SIDE CONNECTOR

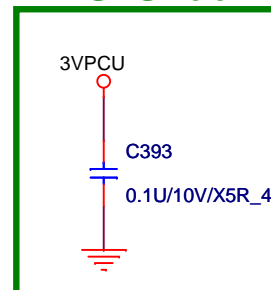
(10,17,21,29,35,37,38,40,41,43) 3VPCU

33

20080928



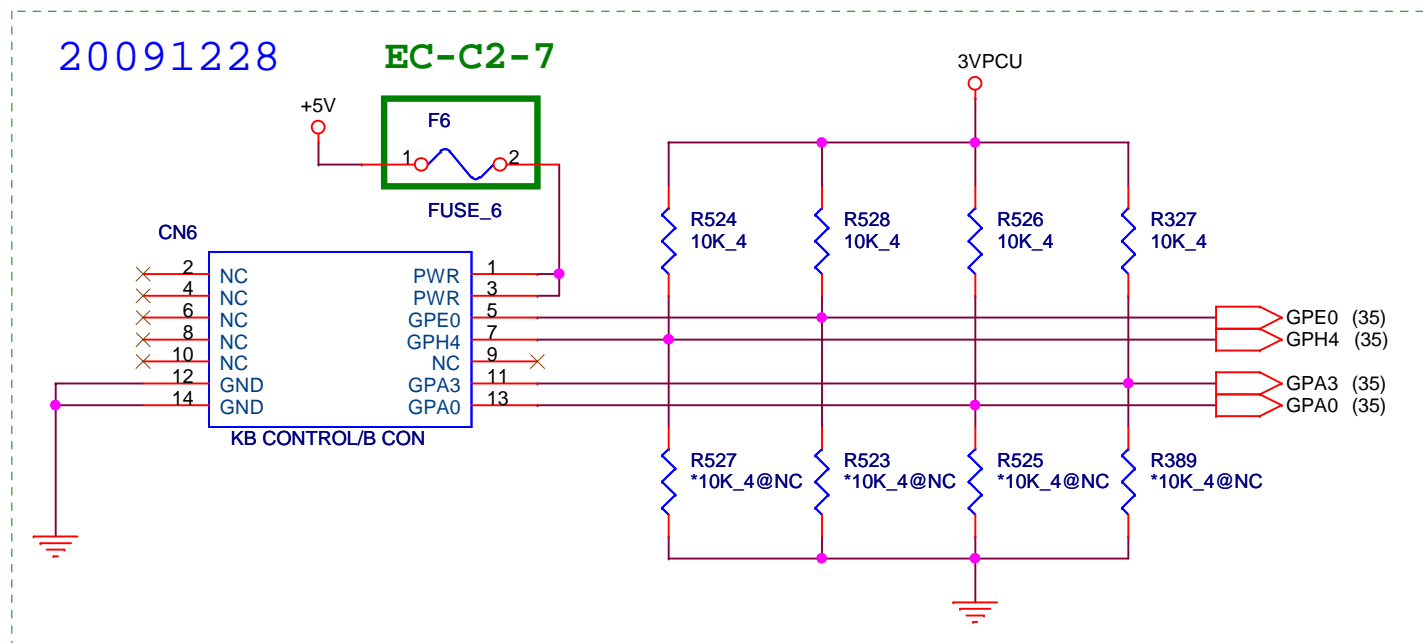
EC-C-60



EC-C-14

20091228

EC-C2-7



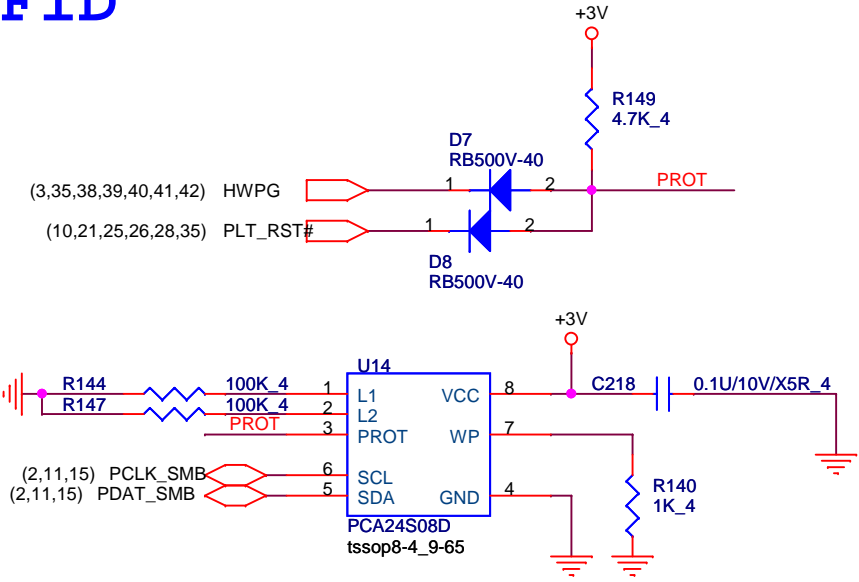
Quanta Computer Inc.


PROJECT :LD-Note AMD UMA

Size	Document Number	Rev
	B TO B CON	1A
Date:	Wednesday, March 31, 2010	Sheet 33 of 49



RFID

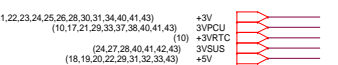


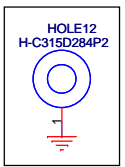
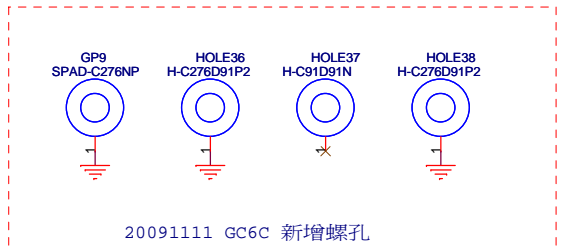
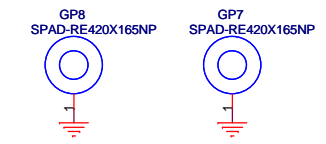
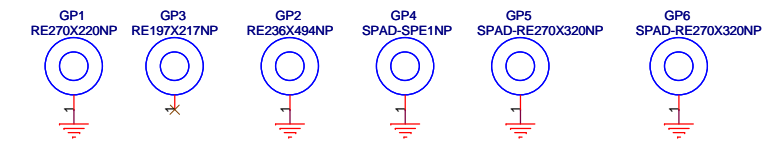
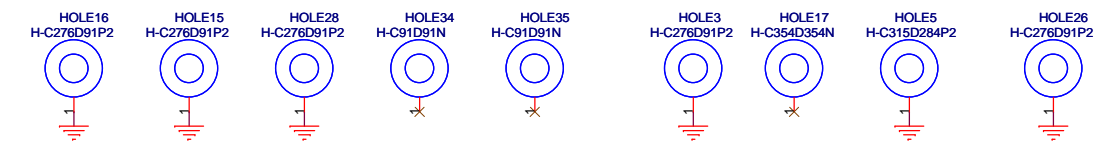
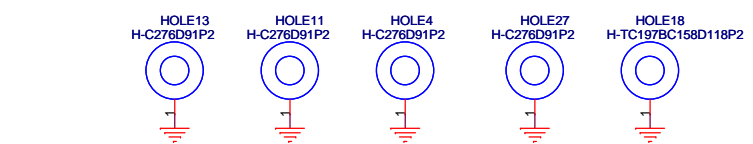
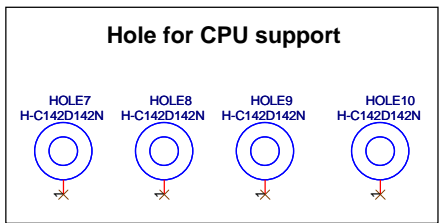
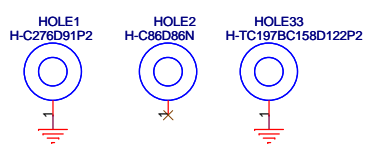
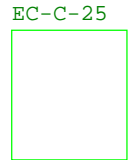
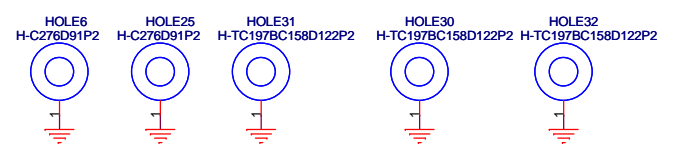
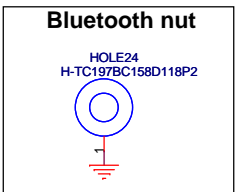
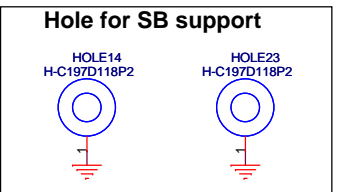
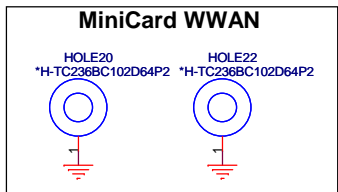
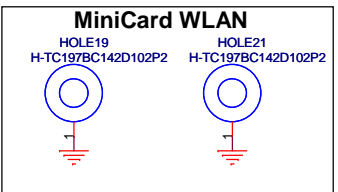


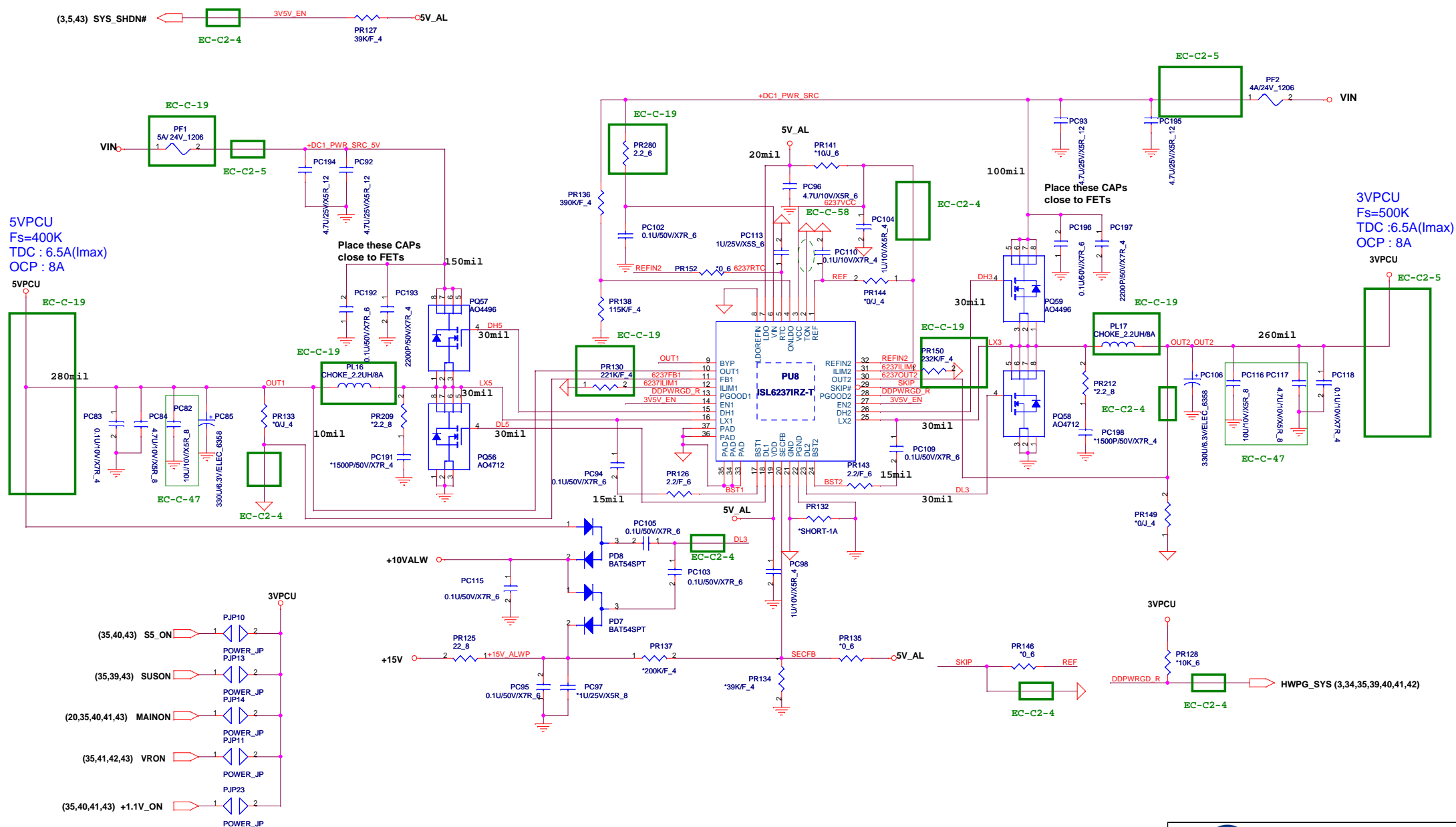
Quanta Computer Inc.

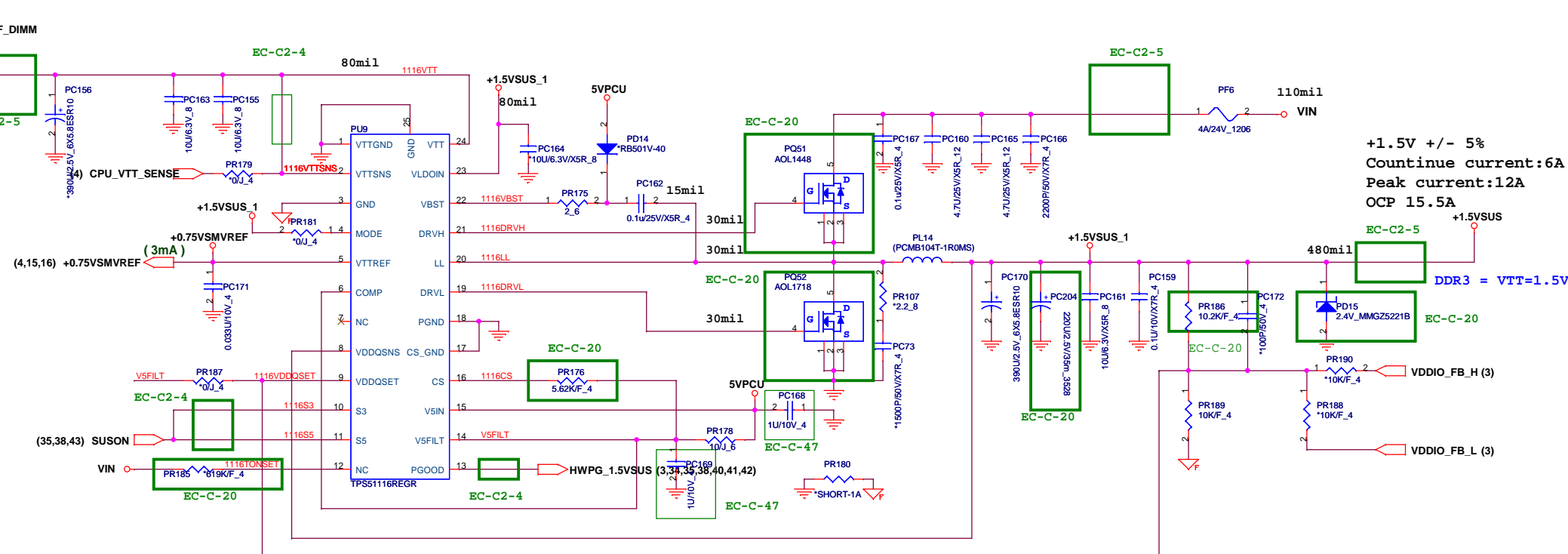
PROJECT :LD-Note AMD UMA

Size	Document Number	Rev 1A
RFID EEPROM		
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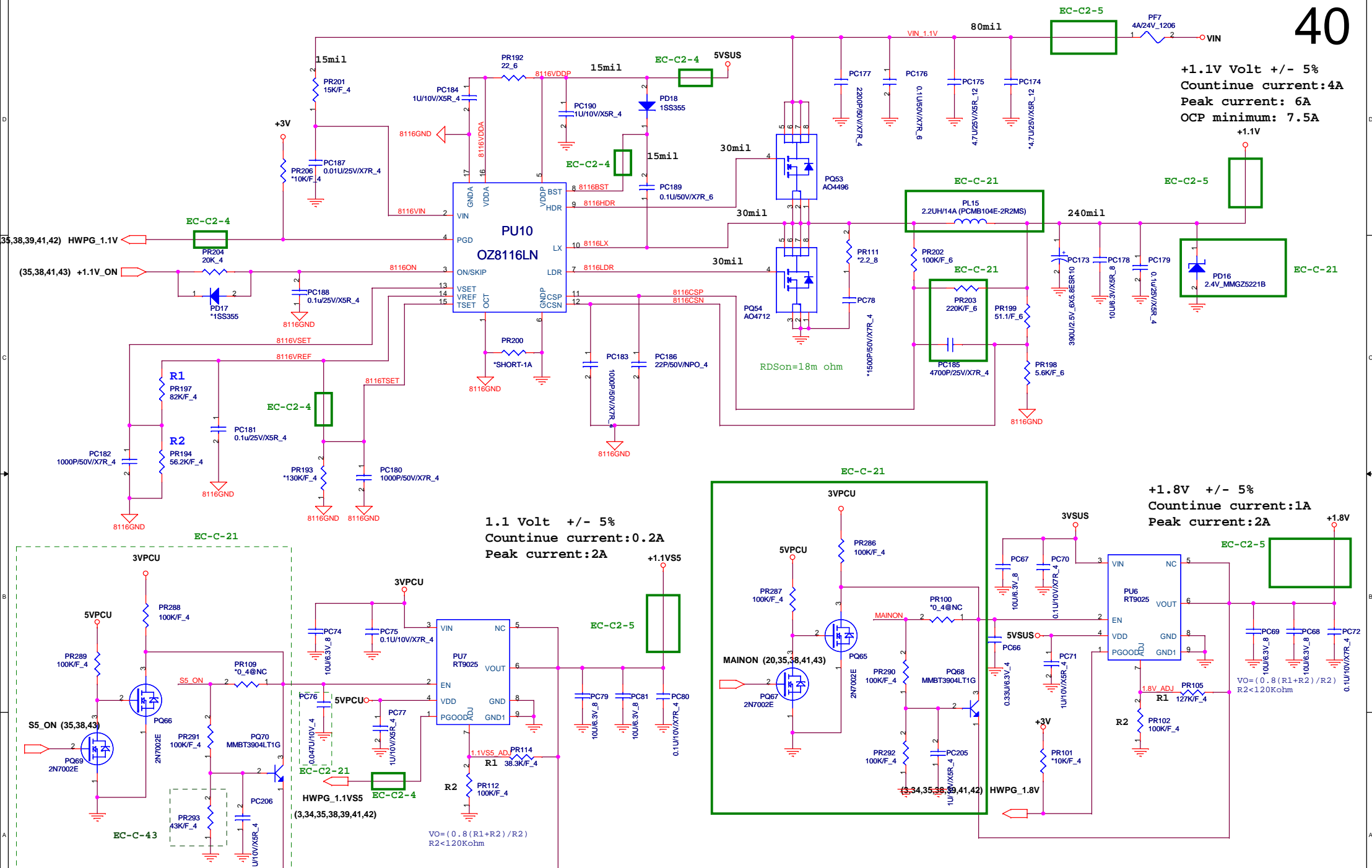








+1.1V Volt +/- 5%
Continue current: 4A
Peak current: 6A
OCP minimum: 7.5A



+1.1V Volt +/- 5%
 Countinue current:6A
 Peak current: 7A
 OCP minimum: 8.7A

+NB_CORE
 NB_CORE = 1.1V

EC-C-11
 EC-C2-5

EC-C-22

+NB_CORE_ON	High	Low
+NB_CORE	0.95	1.1

(B) +NB_CORE_ON

Vo = 0.75 (R1+R2) / R2

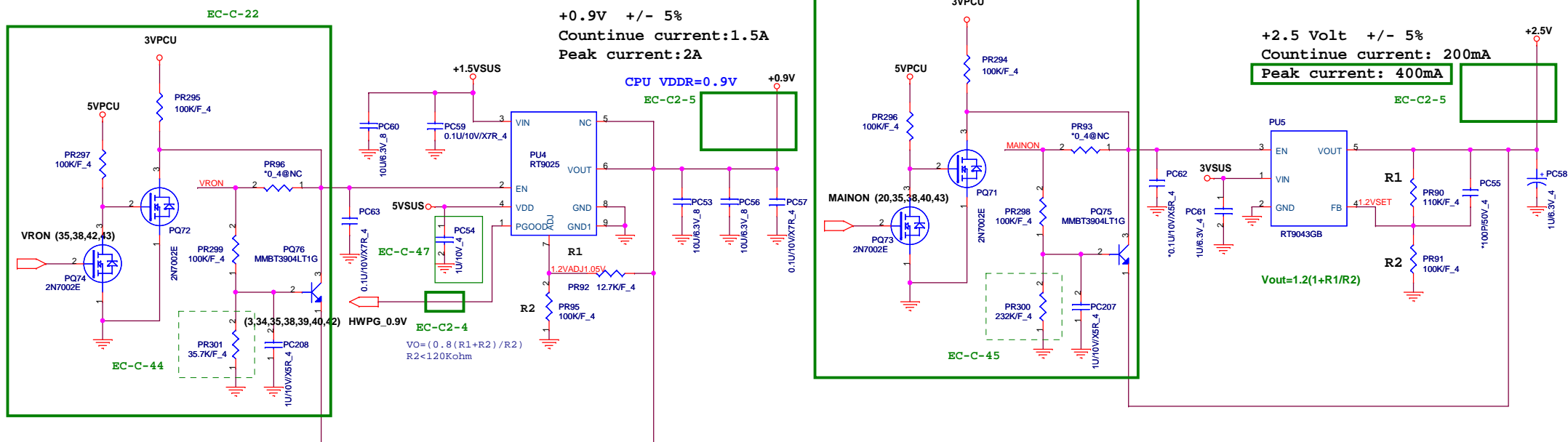
+0.9V +/- 5%
 Countinue current:1.5A
 Peak current:2A

CPU VDDR=0.9V
 EC-C2-5

+2.5 Volt +/- 5%
 Countinue current: 200mA
 Peak current: 400mA

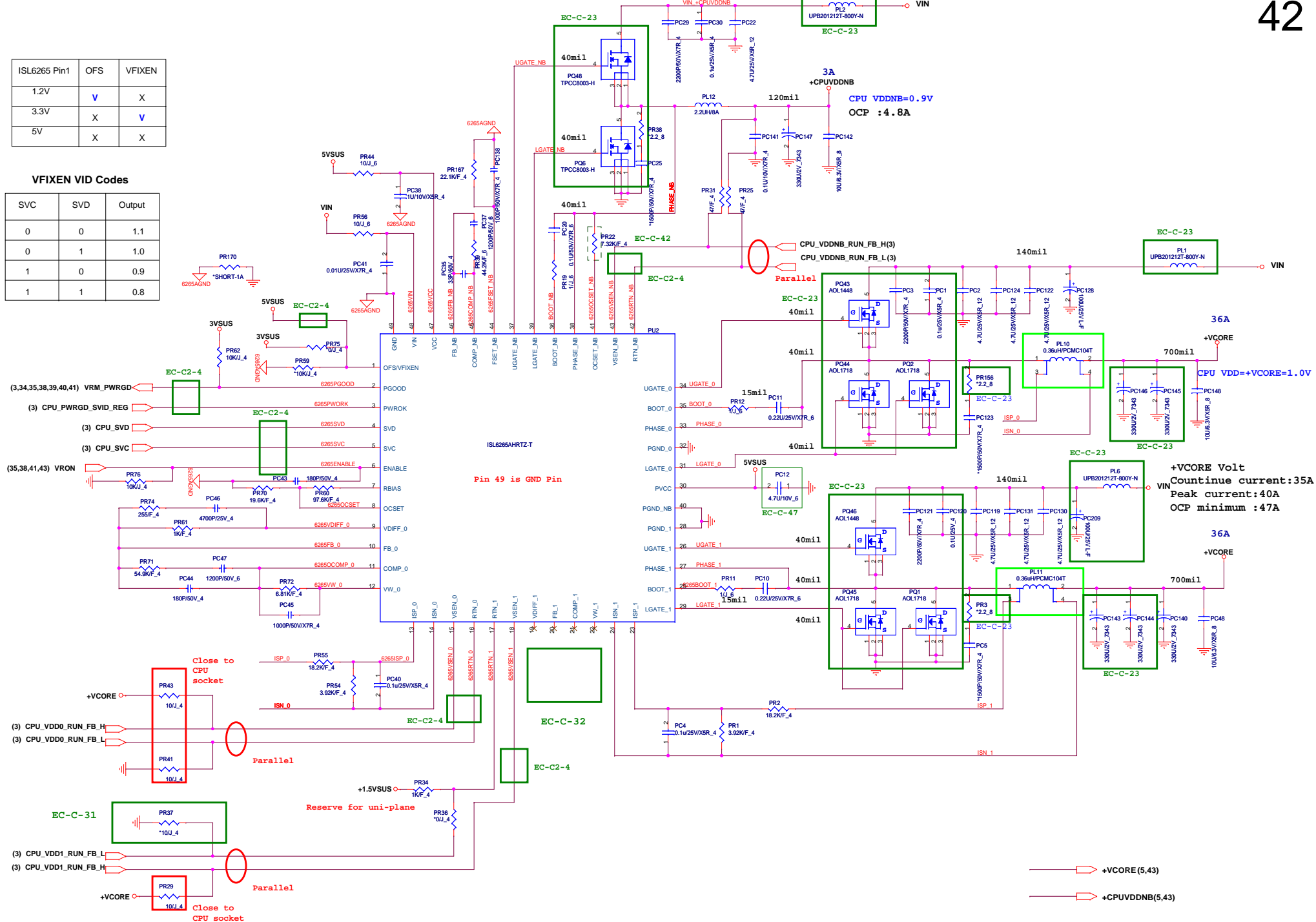
EC-C2-5

Vout=1.2(1+R1/R2)

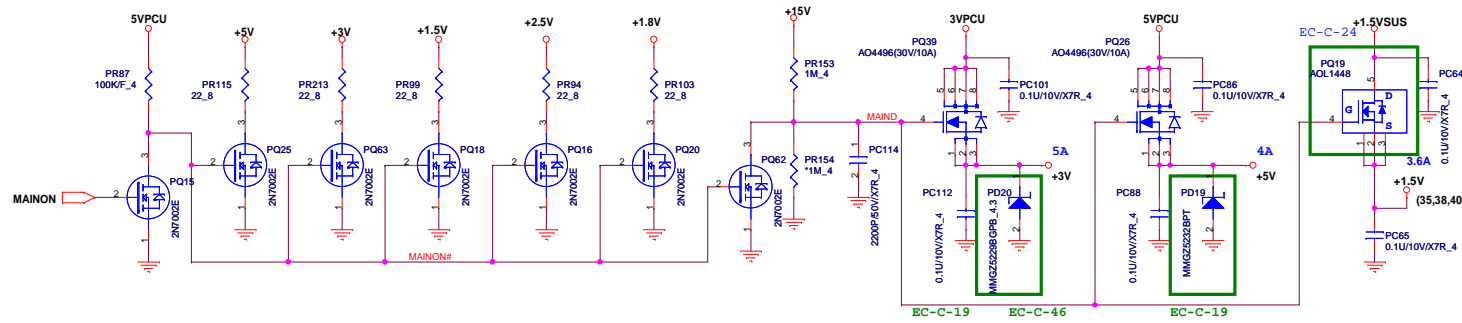


VFIXEN VID Codes

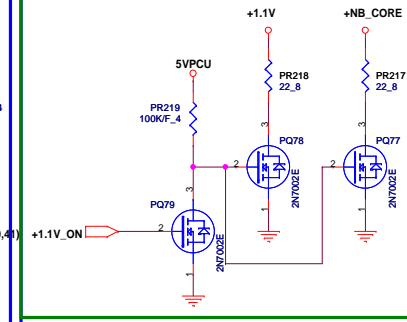
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



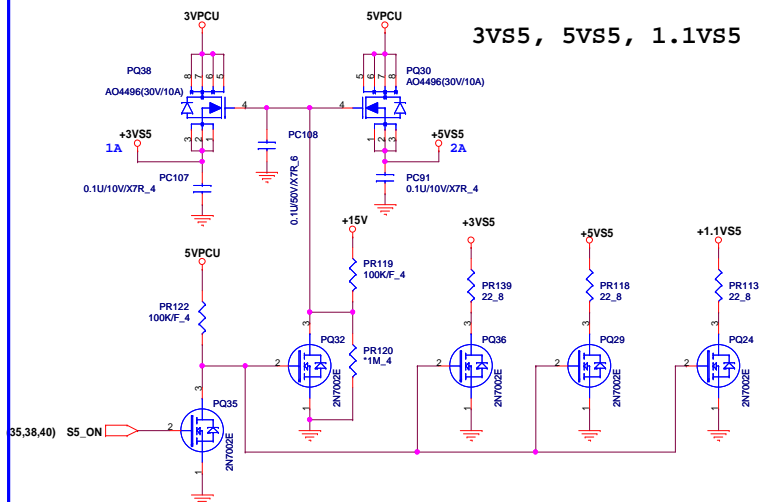
+3V, +5V, +2.5V, +1.8V, +1.5V



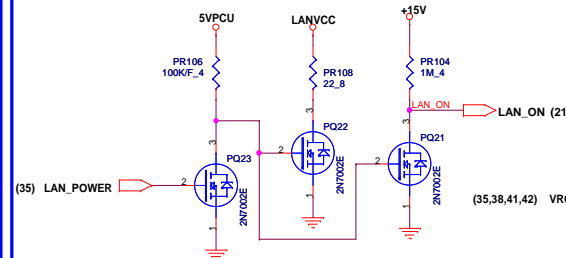
+1.1V, +NB_CORE



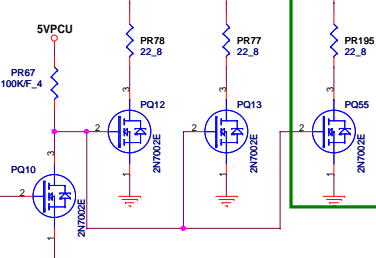
3VS5, 5VS5, 1.1VS5



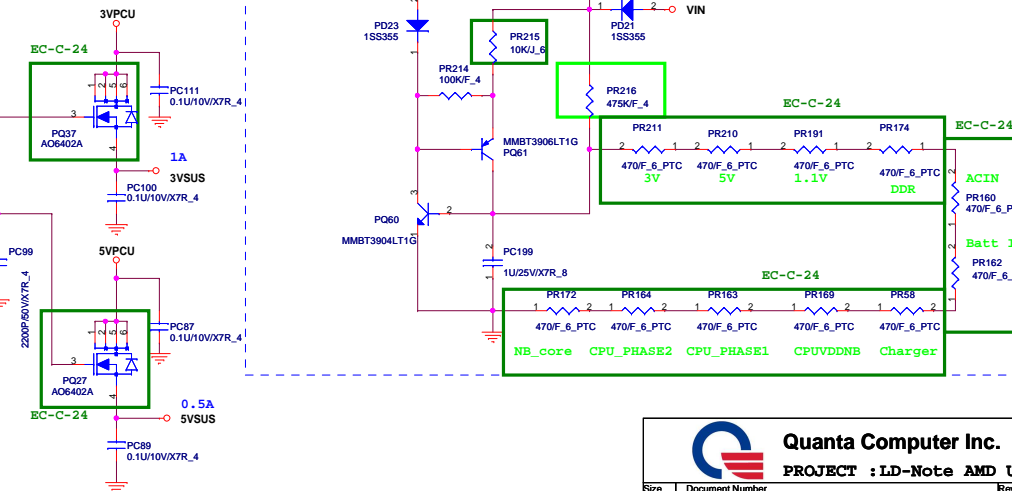
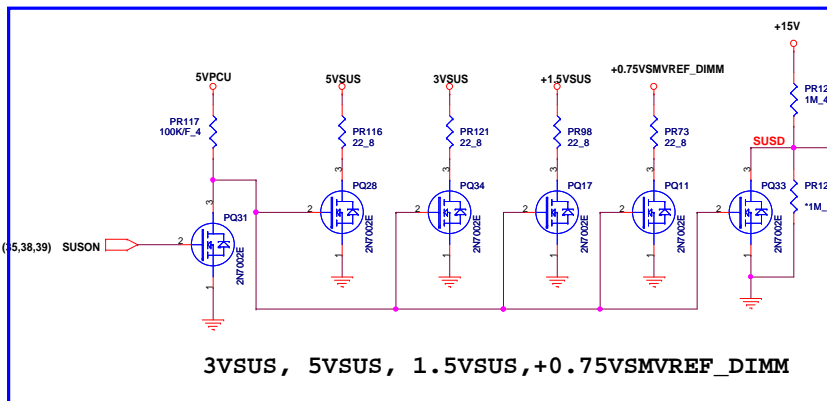
LANVCC



CPU_CORE

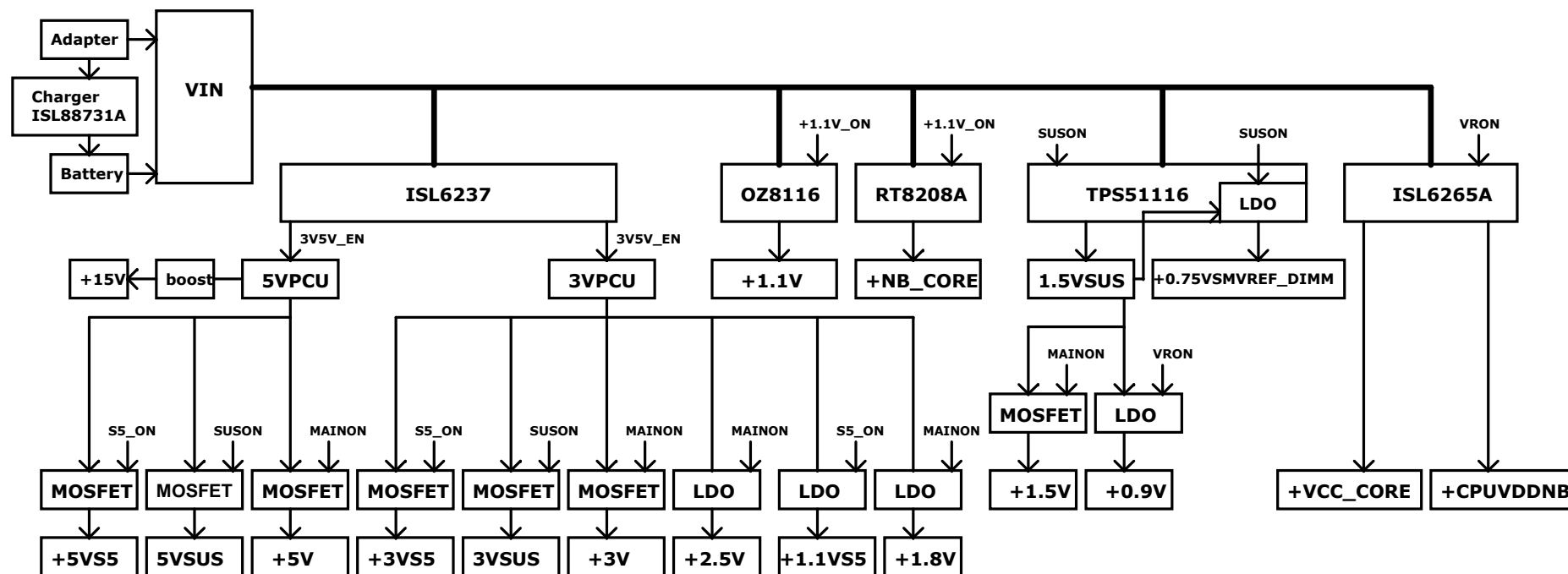


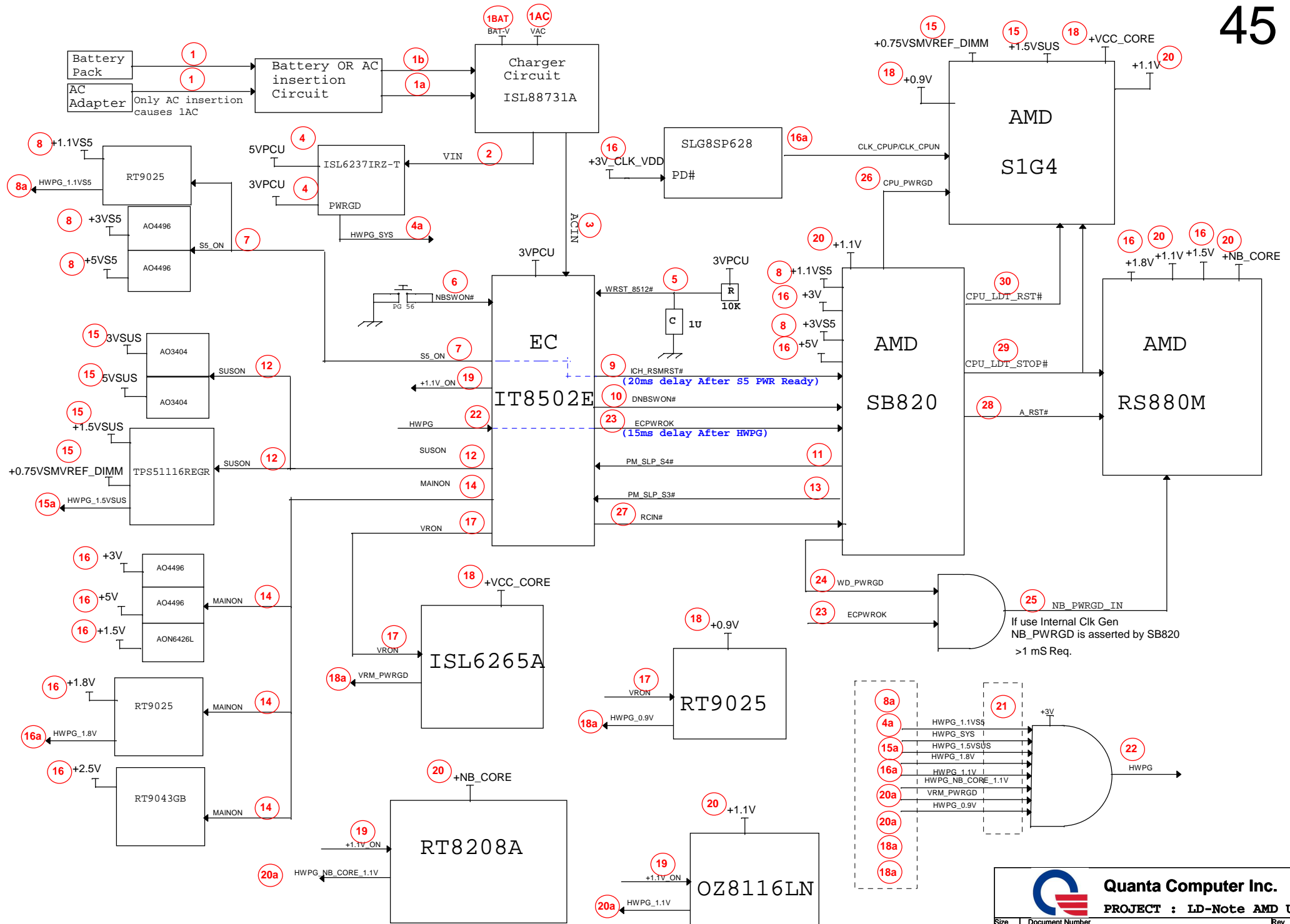
3VSUS, 5VSUS, 1.5VSUS, +0.75VSMVREF_DIMM

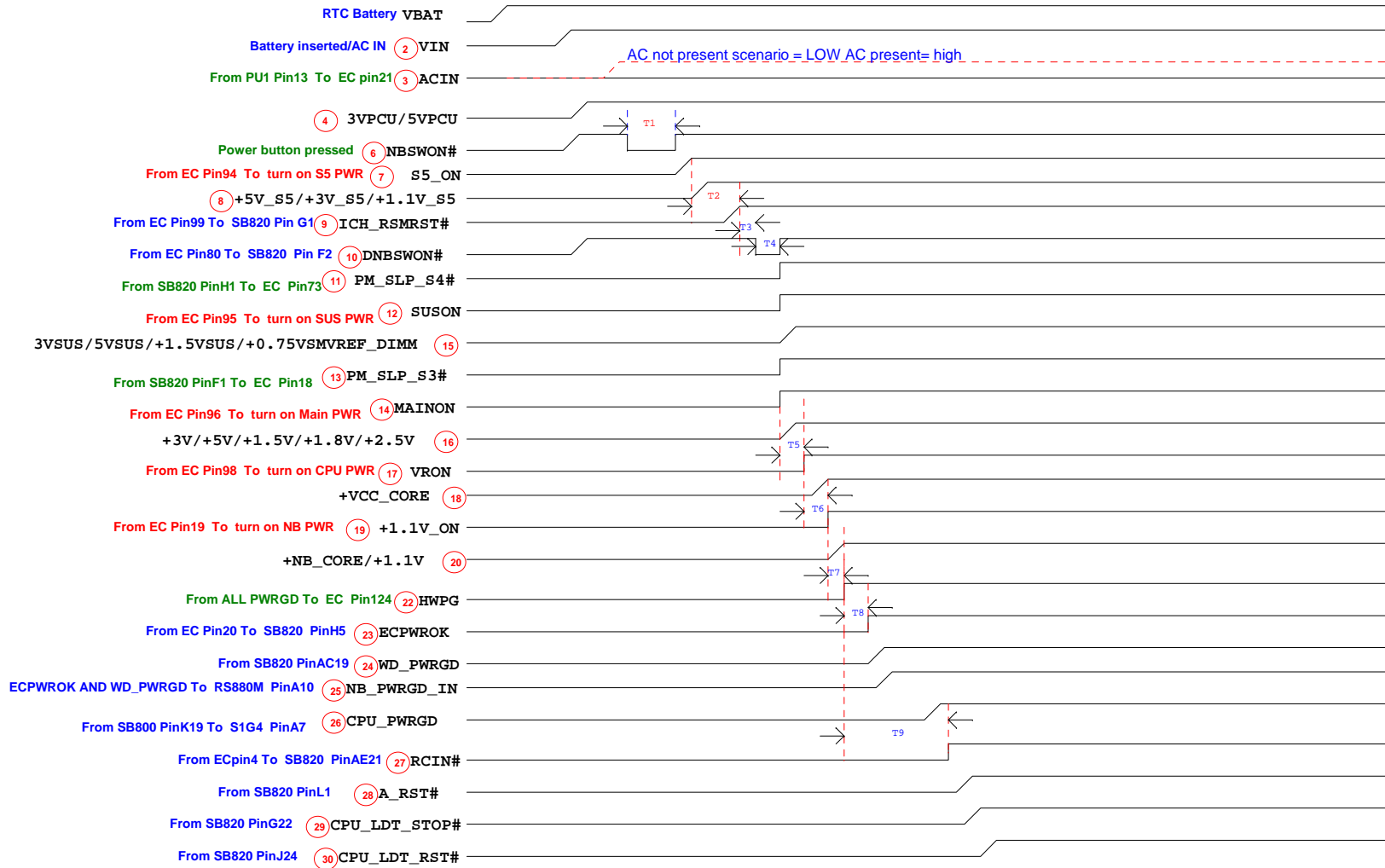


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PROJECT : LD-Note AMD UMA









T1	>16ms
T2	20ms
T3	5ms
T4	1ms
T5	15ms
T6	5ms
T7	5ms
T8	15ms
T9	108ms

EC #	Page	Description	Part Affected
EC-C-01	2	Change Part reference of schematic ,Add L18,L19	L18,L19
EC-C-02	2	Change Part reference of schematic,Add RP4	RP4
EC-C-03	3	Change Part reference of schematic,Add R339,R340,R341 by AMD suggest	R339,R340,R341
EC-C-04	10	Modify layout R478 from U42.1 to U42.2.	U42,R478
EC-C-05	13	Modify layout: Discrete power plane +1.1V_VDDCR and +1.1V_S5VDDCR	U38C
EC-C-06	18	Change BOM 499R --> 715R R192,R194,R196,R199,R201,R206,R216,R220	R192,R194,R196,R199,R201,R206,R216,R220
EC-C-07	20	Change BOM , Add R304,R306 , Del R305,C409 for 1st to 2nd of SDV SMT	Add R304,R306 Del R305,R409
EC-C-08	21	Modify Layout ,Remove ESD Pin5 connect to GND	U13,U16
EC-C-09	27	Change BOM, Add R264 for 1st to 2nd of SDV SMT	R264
EC-C-10	26	Change BOM,and add R250,R253 for 1st to 2nd of SDV SMT	R250,R253
EC-C-11	38 39 40 41	Modify short pad for power trace: short PJP4 , PJP5 ,PJP6 ,PJP7 ,PJP12 ,PJP17 ,PJP18 ,PJP19 ,PJP22	PJP4 , PJP5 ,PJP6 ,PJP7 ,PJP12 ,PJP17 ,PJP18 ,PJP19 ,PJP22
EC-C-12	19	Modify Layout, Add D35	D35
EC-C-13	20	Modify Layout, reserve R529 for POP noise	R529
EC-C-14	33 35	Modify Layout,CN6 Pin11,Pin13,Pin12,Pin14 add resister	CN6 Pin11,Pin13,Pin12,Pin14 R524,R528,R526,R327,R527,R523,R525,R389
EC-C-15	17 21	Change BOM,LED limit current RES value.	R184,R170,R135,R172
EC-C-16	18	Modify Layout,Add R268 Change BOM,Del D13	R268,D13
EC-C-17	18	Modify Layout,Add R530 Change BOM,Del D25	R530,D25
EC-C-18	37	Modify PL3,PL4,PL5,PL8,PL9 source for follow GC5 Modify PQ41,PQ42,PR57 footprint for follow GC5 Modify PF3 rating Add parts for battery learning function and follow GC5 Modify PC134,PC137 for ripple issue	PL3,PL4,PL5,PL8,PL9 PQ41,PQ42,PR57 PF3 PU11,PQ64,PD24,PR281,PR282,PR283,PR284,PR285,PC201,PC202,PC203 PC134,PC137
EC-C-19	38	Modify PR130,PR150 value for OCP adjust Modify PF1,PL16,PL17 for rating issue Add part PR280 for follow GC5 Change PD19,PD20 location for OVP function	PR130,PR150 PF1,PL16,PL17 PR280 PD19,PD20
EC-C-20	39	Modify PQ51,PQ52 footprint for follow GC5 Modify PR176 value for OCP adjust Add part PC204 for ripple issue Modify PR186 value for output voltage adiust and follow GC5 PD15 POP,PR185 DEPOP	PQ51,PQ52 PR176 PC204 PR186 PD15,PR185
EC-C-21	40	Modify PL15 type Modify PR203,PC185 value for OCP adjust PD16 POP Add parts for UVP function and follow GC5	PL15 PR203,PC185 PD16 PQ65,PQ66,PQ67,PQ68,PQ69,PQ70,PR286,PR287,PR288,PR289,PR290,PR291,PR292,PR293,PC205,PC206
EC-C-22	41	Modify PL13 type PD13 POP Add parts for UVP function and follow GC5	PL13 PD13 PQ71,PQ72,PQ73,PQ74,PQ75,PQ76,PR294,PR295,PR296,PR297,PR298,PR299,PR300,PR301,PC207,PC208
EC-C-23	42	Modify footprint for follow GC5 Modify PC143,PC144,PC145,PC146 type Add part PC209 Modify PR3,PR156 value PL1,PL2,PL6 POP	PQ1,PQ2,PQ6,PQ43,PQ44,PQ45,PQ46,PQ48 PC143,PC144,PC145,PC146 PC209 PR3,PR156 PL1,PL2,PL6
EC-C-24	43	Modify PQ19,PQ27,PR37 rating for extended combustion issue and follow GC5 Modify PR58,PR160,PR162,PR163,PR164,PR169,PR172,PR174,PR191,PR210,PR211 Add part for discharge	PQ19,PQ27,PR37 PR58,PR160,PR162,PR163,PR164,PR169,PR172,PR174,PR191,PR210,PR211 PQ55,PQ77,PQ78,PQ79,PR195,PR217,PR218,PR219
EC-C-25	35	D11,D12,D14,D15,D16,D17,D18,D19 change to R537,R538,R39,R540,R541,R542,R543,R544	D11,D12,D14,D15,D16,D17,D18,D19 R537,R538,R39,R540,R541,R542,R543,R544
EC-C-26	17,23,24	Add Common choke for EMI issue.	CML1, R233, R235, CML2, R402, R405 CML3, R448, R449 CML4, R503, R504 L22, R176, R179
EC-C-27	7	Remove component for HDMI EA test	R366, R368, R371, R374
EC-C-28	8	For EA Clock test issue, change footprint shortpad to normal 0420 size pad of R533 and R537. Add R535 and R536 for Internal clock switch(SIT BOM not mount).	R533 R537, R535, R536
EC-C-29	21 2 12 10	Modify Crystal capcitor value to reache ideal frequency	Y1, C187, C188 Y2, C213, C221 Y6, C587, C548 Y8, C583, C584

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